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Effect of an inserted Al_2O_3 passivation layer for atomic layer deposited HfO_2 on indium phosphide

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Abstract

In this study, we demonstrate indium phosphide (InP) metal–oxide–semiconductor capacitors (MOSCAPs) with single HfO_2 and stacked HfO_2/Al_2O_3 dielectrics. Based on these capacitors, the effect of an inserted Al_2O_3 passivation layer with various thicknesses on the properties of InP MOSCAPs was further statistically investigated. By inserting a 2 nm thick Al_2O_3 passivation layer between high-κ HfO_2 and the InP substrate, the characteristics including the frequency dispersion, leakage current and interface trap density (D_{it}) were effectively improved, which could be attributed to the large bandgap of Al_2O_3 that suppressed substrate element diffusion and reduced oxidation of the InP substrate. A low D_{it} of $\sim 3.8 \times 10^{11}$ cm^{-2} eV^{-1} that was comparable to that of previously reported InP MOSCAPs was achieved. However, with the thickness of Al_2O_3 decreasing from 2 to 1 nm, the frequency dispersion and D_{it} were slightly increased, because such an ultrathin Al_2O_3 layer could not effectively suppress the diffusion and may induce substrate oxidation after annealing. The present results show that the incorporation of an Al_2O_3 passivation layer with suitable thickness has great promise in future high-performance InP device applications.

Keywords: InP, capacitor, passivation, interface trap density

(Some figures may appear in colour only in the online journal)

1. Introduction

As silicon-based technology has reached its physical limits, III–V semiconductors have been extensively investigated, especially for low-power and high-frequency device applications, because of their high electron mobility and wide bandgap [1, 2]. Indium phosphide (InP) is considered to be one of the most promising candidates among III–V semiconductors due to its high electron mobility ($\sim$5000 cm^2 V^{-1} s^{-1}), large bandgap ($\sim$1.34 eV) and direct-gap property [3, 4]. Simultaneously, since the reduction of silicon oxide thickness may make insulation for the continuous scaling of complementary metal–oxide–semiconductor (MOS) devices to deep nanotechnology invalid, the use of a high-permittivity (high-κ) dielectric as an alternative to silicon oxide for enhancing the performance of MOS devices has attracted much attention [5–9]. HfO_2 has been found to be a suitable dielectric for use in electronic devices with high permittivity ($\sim$25), as it can maintain insulation with a small equivalent oxide thickness [10]. However, compared with the ultra-high adaptability between silicon and its natural oxide, the poor interface between the high-κ oxide and semiconductor, such as lattice mismatch, lattice defects, interface impurities and many dangling bonds, leads to an increase in interface trap density (D_{it}) which has a serious influence on device performance; this has become one of the main topics in fabrication of high-performance III–V devices. Therefore, many researchers have looked at improving the

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interface quality between the III–V semiconductor substrate and the high-κ oxide and many approaches have been reported, including treating the semiconductor surface chemically, using different annealing conditions, changing the dielectric layer material and designing a stacked structure [9, 11–32]. Among the solutions proposed above, a stacked structure has been widely studied as an effective method in both silicon and compound semiconductors. Recently, Al_2O_3 has been proved to suppress elemental diffusion from the substrate when used as a passivation layer [24–31]. The dielectric constant of Al_2O_3 is about twice that of SiO_2, so it can keep the equivalent oxide thickness small. O'Mahony reported a GaAs metal–oxide–semiconductor capacitor (MOSCAP) with Al_2O_3 as the interface control layer that exhibited an improved interface quality with reduced leakage current density and frequency dispersion [23]. Mahata also reported that Al_2O_3 passivation could effectively prevent significant incorporation of In in high-κ film and reduce D_{it} in an InGaAs MOSCAP [24].

In this work, based on a number of randomly selected InP MOSCAPs, we investigated the effect of an inserted Al_2O_3 passivation layer with various thicknesses on the properties of InP MOSCAPs. By inserting an Al_2O_3 layer with appropriate thickness between HfO_2 and the InP substrate, good characteristics, including low frequency dispersion, low leakage current and low D_{it} with a magnitude of $\sim 10^{11}$ cm^{-2} eV^{-1}, were achieved; this could be beneficial for future applications of high-performance InP devices.

2. Experiments

The InP MOSCAPs were fabricated on sulfur-doped n-type (100) InP wafers with a carrier concentration of $\sim 1 \times 10^{17}$ cm^{-3}. First, the InP substrate was cleaned with acetone, alcohol and deionized water in an ultrasonic bath (5 min each), followed by cleaning with diluted HF solution for 5 min to remove the native oxide. After surface cleaning, the dielectric stacks with 1 or 2 nm thick Al_2O_3 and 4 nm thick HfO_2 were formed by atomic layer deposition using $[(CH_3)_3Al]_2$ (TMA) and $Hf[N(CH_3)(C_2H_5)]_4$ (TDMAH) as precursors and water vapor as the oxidant at 200 °C, followed by post-deposition annealing (PDA) at 400 °C for 10 min in a N_2 ambient. For comparison, a control sample with a single 6 nm thick HfO_2 dielectric was also fabricated to investigate the effect of an inserted Al_2O_3 passivation layer. Finally, a 20/100 nm thick Cr/Au metal layer was deposited by magnetron sputtering and patterned by a shadow mask as the gate electrode. For the measurement, the electrical performance including the capacitance–voltage (C–V) and current–voltage (I–V) properties were characterized using an Agilent E4980A precision LCR meter and 4156C semiconductor device analyzer, respectively, at room temperature. The chemical bonding state was analyzed by x-ray photoelectron spectroscopy (XPS).

3. Results and discussion

Figure 1(a) presents the schematic structure of the fabricated InP MOSCAPs with an HfO_2/Al_2O_3 dielectric stack

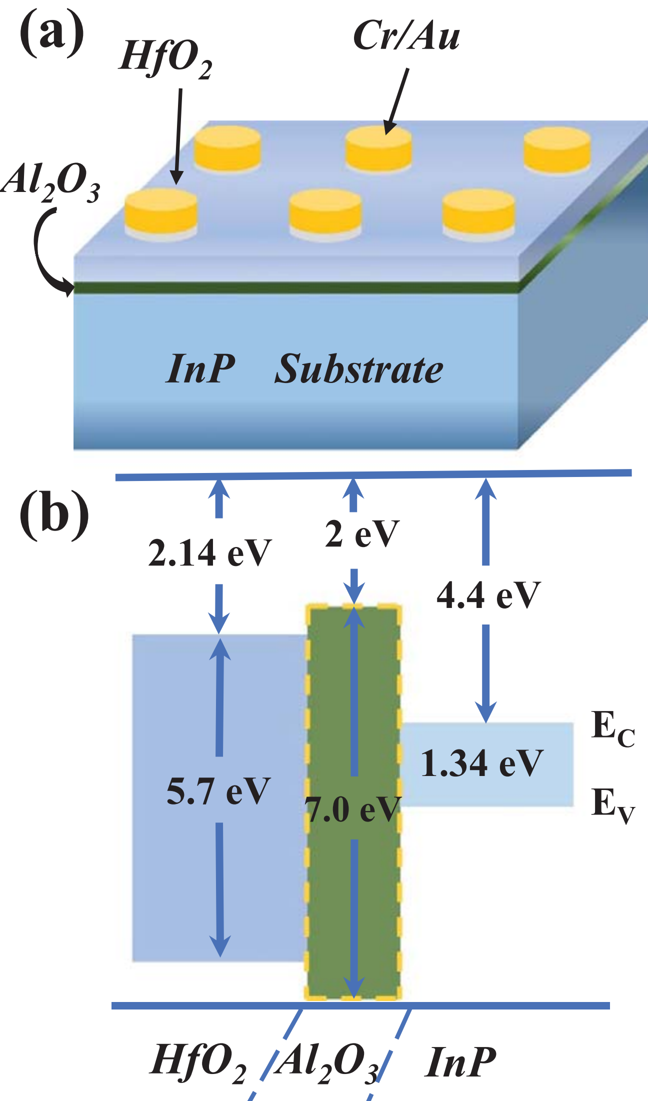


Figure 1. (a) Schematic structure and (b) band diagram of the HfO_2/Al_2O_3/InP MOSCAP.

and Cr/Au gate electrodes. The gate electrodes have a radius of 60 μm. Figure 1(b) reveals the band diagram of the HfO_2/Al_2O_3/InP MOSCAP, which was obtained according to the bandgaps and electron affinities of InP, Al_2O_3 and HfO_2 materials. The bandgaps of InP, Al_2O_3 and HfO_2 are $\sim$1.34, $\sim$7.0 and $\sim$5.7 eV [4, 10, 22], respectively, while the electron affinities of InP, Al_2O_3 and HfO_2 are $\sim$4.4, $\sim$2.0 and $\sim$2.14 eV [33, 34], respectively. Although HfO_2 has the advantage of high permittivity, it may cause a leakage current due to the small conduction band offset with the InP substrate. Therefore, to solve the dilemma between the bandgap and permittivity of a single HfO_2 dielectric, a stacked dielectric that consists of high-permittivity HfO_2 and Al_2O_3 which has a large bandgap could be a good candidate. From figure 1(b), it can be seen that Al_2O_3/InP offers a larger conduction band offset than HfO_2/InP, which could contribute to a lower gate leakage current and further enhance the interface quality and device performance. It has been reported that atomic layer

deposited Al_2O_3 could effectively suppress substrate oxidation and atom diffusion, which could be ascribed to the good quality of the Al_2O_3/semiconductor interface [9, 24–26].

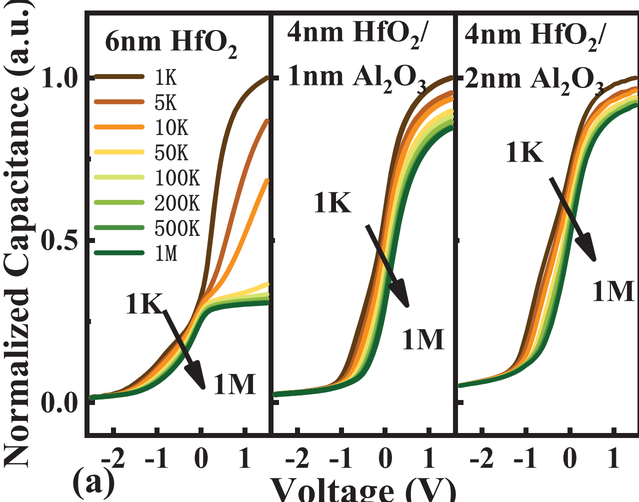
Figure 2(a) shows the normalized *C*–*V* curves of the InP MOSCAPs with a single 6 nm HfO_2 dielectric, 4 nm HfO_2/1 nm Al_2O_3 and 4 nm HfO_2/2 nm Al_2O_3 at various frequencies and room temperature, respectively. The *C*–*V* characteristics were measured at various frequencies from 1 kHz to 1 MHz in a DC sweeping voltage range from −2.5 to 1.5 V. The *C*–*V* curves of all the InP MOSCAPs exhibited accumulation in the direction of positive voltage and deep depletion in the direction of negative voltage. A trap response time (τ) of 12.5 μs was obtained from the Shockley–Read–Hall statistics of capture and emission rates according to the equation [5, 35]

$$\tau = 2 \times \frac{\exp\left[\frac{E_C - E_V}{2k_B T}\right]}{\sigma v_{th} D_{dos}} \tag{1}$$

where $v_{th} = (3k_B T/m^*)^{1/2}$ is the average thermal velocity of the majority carriers, T is the temperature, k_B is the Boltzmann constant, m^* is majority carrier effective mass, σ is the capture cross section of the trap with a typical magnitude from 10^{-12} to 10^{-16} cm^2, $D_{dos} = 2(3\pi m^* k_B T/h^2)^{3/2}$ is the equivalent density of states of the majority carrier band, h is the Planck constant and E_c and E_v are the conduction and valence band energies, respectively. On the other hand, the time to form an inversion (τ_{inv}) can be calculated by [36]

$$\tau_{inv} = \frac{2N_D \tau}{n_i} \tag{2}$$

where n_i and N_D are the intrinsic carrier concentration and doping concentration of the InP, respectively. A large τ_{inv} of 760 s was obtained, indicating that formation of an inversion was impossible in this study. A similar phenomenon has also been observed in previous reports [14, 18, 30]. It can be clearly seen that frequency dispersion occurred in all the InP MOSCAPs, as shown in figure 2(a), as was often found on a compound substrate [20, 21]. The amount of frequency dispersion was defined as the percentage ratio of the change in maximum capacitance (C_{max}) measured from 1 kHz to 1 MHz [12]. Here, C_{max} was measured at a gate voltage of 1.5 V. Compared with the MOSCAP with a single 6 nm HfO_2 dielectirc, the MOSCAP with stacked 4 nm HfO_2/2 nm Al_2O_3 exhibited better frequency dispersion in the accumulation region. This indicates the better interface quality produced by inserting an Al_2O_3 layer with large bandgap between HfO_2 and the InP substrate, as shown in figure 1(b). With the scaling down trend, the thickness of the inserted Al_2O_3 was reduced to 1 nm, resulting in a higher oxide capacitance but degraded frequency dispersion in the accumulation region. This degradation could be explained by the disorder-induced gap state model [37, 38]. Such an ultrathin Al_2O_3 layer could not effectively suppress diffusion from the substrate, which may result in substrate oxidation [8, 31]. The carriers resulting from the oxidation tunneled into the disordered region, causing frequency dispersion. In order to avoid the deviation caused



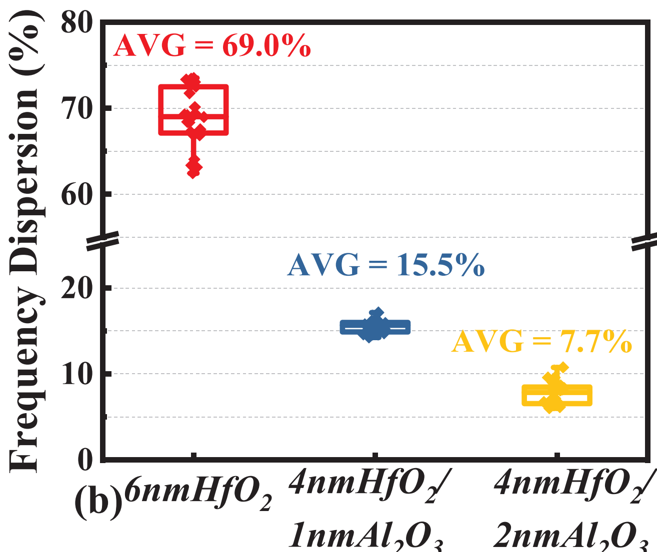


Figure 2. (a) Normalized *C*–*V* curves of the InP MOSCAPs with a single 6 nm HfO_2 dielectric, 4 nm HfO_2/1 nm Al_2O_3 and 4 nm HfO_2/2 nm Al_2O_3 at various frequencies. (b) Frequency dispersion of the randomly selected MOSCAPs with single and stacked dielectrics.

by a single sample and observe the statistical laws reflected in multiple test samples, 25 samples from each of the three types of InP MOSCAP were selected at random and tested. Figure 2(b) shows the frequency dispersion of the randomly selected MOSCAPs with single and stacked dielectrics. Average frequency dispersions of 69.0%, 15.5% and 7.7% were obtained for the InP MOSCAPs with a single 6 nm HfO_2 dielectric, 4 nm HfO_2/1 nm Al_2O_3 and 4 nm HfO_2/2 nm Al_2O_3, respectively. It was observed that the MOSCAP with a single 6 nm HfO_2 dielectric exhibited much higher frequency dispersion and worse uniformity, in agreement with the discussion above. These results show that inserting a relatively thick oxide layer with large bandgap between the high-κ material and the InP substrate could improve the interface quality by reducing the frequency dispersion. In addition, all the InP MOSCAPs in this work exhibited a *C*–*V* hysteresis property

with a hysteresis offset of ∼0.5 V (not shown here), which was also commonly reported in previous publications [13–15]. Further studies on improving the hysteresis characteristic are needed.

To further investigate the effect of Al_2O_3 passivation quantitatively, the Castagné–Vapaille method, which has been commonly used in III–V MOSCAPs, was utilized to evaluate the D_{it} distribution according to the following equation [14, 22]:

$$D_{it} = \frac{C_{ox}}{q}\left(\frac{C_{lf}/C_{ox}}{1 - C_{lf}/C_{ox}} - \frac{C_{hf}/C_{ox}}{1 - C_{hf}/C_{ox}}\right) \tag{3}$$

where C_{ox} is the oxide capacitance (maximum capacitance in accumulation), C_{lf} is the low-frequency capacitance at 1 kHz, C_{hf} is the high-frequency capacitance at 1 MHz and q is the electron charge. With equation (3), the relation between D_{it} and gate voltage (V_g) could be obtained. However, in order to evaluate the distribution of D_{it} with the energy bandgap, it is necessary to convert V_g to surface potential (ψ_s). The classic conversion method used the depletion of surface potential approximation as follows [5, 22]:

$$\psi_s = \frac{\varepsilon_s \varepsilon_0 q N_D}{2C_s^2} \tag{4}$$

$$\frac{1}{C_s(V_g)} = \frac{1}{C_m(V_g)} - \frac{1}{C_{ox}} \tag{5}$$

$$E - E_i = qV_B - \psi_s \tag{6}$$

where ε_S is the semiconductor dielectric constant, ε_0 is the permittivity of free space, N_D is the doping concentration in the substrate, C_s is the semiconductor capacitance, including the capacitance of interface traps, C_m is the measured capacitance, E is the interface trap energy level, E_i is the midgap of the semiconductor band and qV_B is the bulk potential of the semiconductor. Taking the flatband voltage (V_{FB}) as the reference, the V_g–ψ_s conversion in the depletion region used equations (4) and (5), while the conversion in the accumulation region used the accumulation of surface potential approximation [39]:

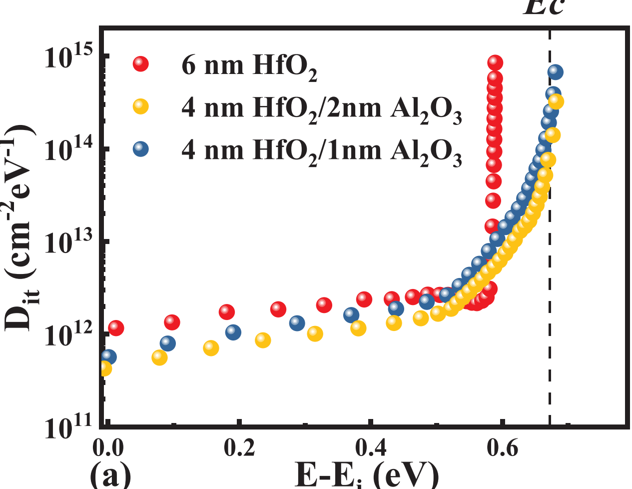
$$\psi_s = \frac{2kT}{q} \times ln\left(\sqrt{\frac{\varepsilon_s \varepsilon_0 q N_D}{kT/q}} \times \frac{1}{C_s}\right). \tag{7}$$

V_{FB} could be obtained by calculating the flatband capacitance (C_{FB}) from the 1 MHz C–V plot as [14]

$$C_{FB} = \frac{C_{ox}}{1 + \frac{\varepsilon_{ox} L_D}{\varepsilon_s d}} \tag{8}$$

$$L_D = \sqrt{\frac{\varepsilon_{ox}\varepsilon_s k_B T}{q^2 N_D}} \tag{9}$$

where L_D is the Debye length. Based on equations (4)–(9), the D_{it} distribution of the InP MOSCAPs with a single 6 nm HfO_2 dielectric, 4 nm HfO_2/1 nm Al_2O_3 and 4 nm HfO_2/2 nm Al_2O_3 was extracted and is shown in figure 3(a). The D_{it} distribution exhibited a U-shaped trend with its minimum at the midgap and maximum near E_c, which is commonly found in classic n-type III–V semiconductor MOSCAPs [20, 25, 26]. It was observed that the extracted D_{it} for the InP MOSCAPs with different dielectrics was in good agreement with the frequency dispersion above. After inserting the Al_2O_3 layer between HfO_2 and the InP substrate, D_{it} was improved due to Al_2O_3 passivation, which could prevent the out-diffusion of both In and P atoms and suppress substrate oxidation [25, 28, 31]. Additionally, with increasing Al_2O_3 thickness, D_{it} was further improved slightly, which may ascribed to the effective prevention of elemental diffusion from the substrate and substrate oxidation after PDA. Figure 3(b) depicts the D_{it} of the randomly selected MOSCAPs with single and stacked dielectrics (25 devices each). The average D_{it} at the midgap of the



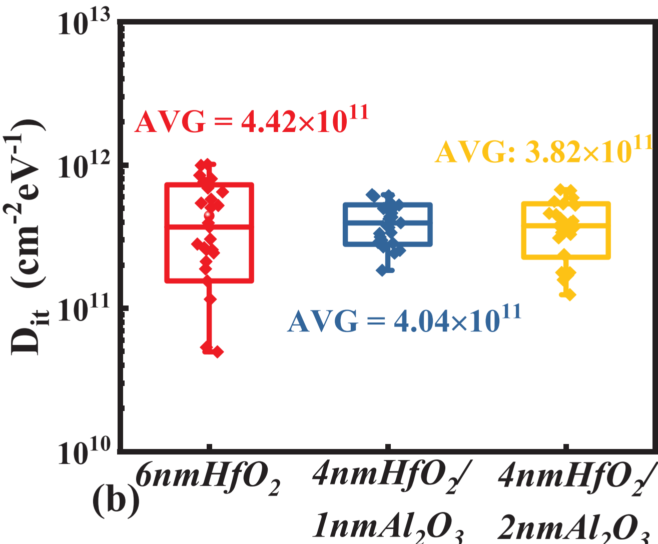


Figure 3. (a) D_{it} distribution of the InP MOSCAPs with a single 6 nm HfO_2 dielectric, 4 nm HfO_2/1 nm Al_2O_3 and 4 nm HfO_2/2 nm Al_2O_3, (b) D_{it} of the randomly selected MOSCAPs with single and stacked dielectrics.

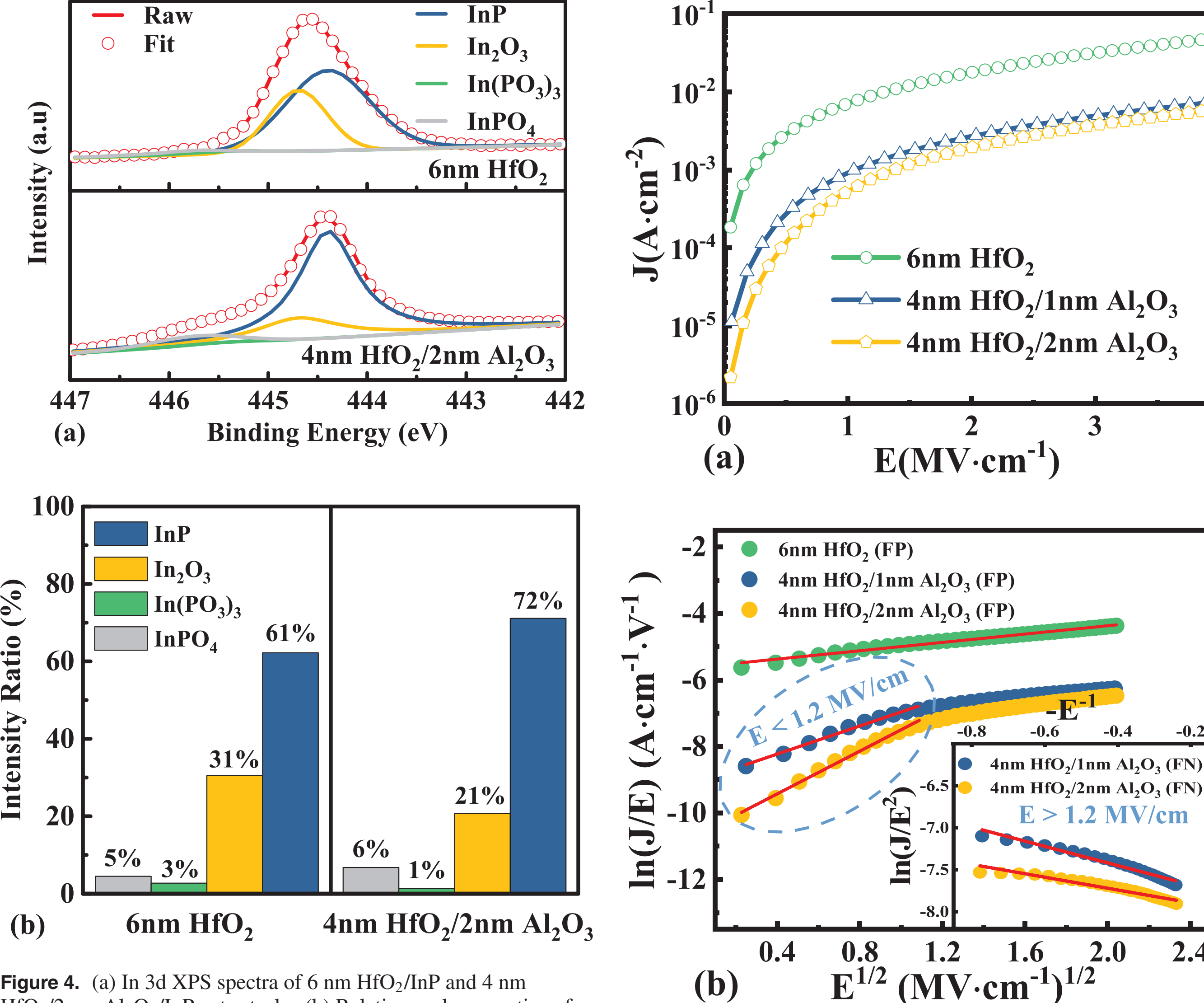


Figure 4. (a) In 3d XPS spectra of 6 nm HfO_2/InP and 4 nm HfO_2/2 nm Al_2O_3/InP gate stacks. (b) Relative peak area ratios of the various components.

Figure 5. (a) *J*–*E* characteristics and (b) current fitting of the InP MOSCAPs with a single 6 nm HfO_2 dielectric, 4 nm HfO_2/1 nm Al_2O_3 and 4 nm HfO_2/2 nm Al_2O_3.

InP MOSCAPs with a single 6 nm HfO_2 dielectric, 4 nm HfO_2/1 nm Al_2O_3 and 4 nm HfO_2/2 nm Al_2O_3 was 4.4×10^{11}, 4.0×10^{11}, 3.8×10^{11} cm^{-2} eV^{-1}, respectively. These results also indicated that an appropriate thickness of the Al_2O_3 passivation layer can effectively improve the interface quality.

To further investigate the mechanism of the inserted Al_2O_3 passivation layer, XPS analysis was performed to study the interfacial chemical states of the gate stacks. Figure 4(a) shows the In 3d XPS spectra of the 6 nm HfO_2/InP and 4 nm HfO_2/2 nm Al_2O_3/InP gate stacks. The binding energy was corrected by referencing the C 1s peak at 284.8 eV. The In 3d spectra were deconvoluted into four sub-peaks including InP, In_2O_3, $In(PO_3)_3$ and $InPO_4$ with the binding energies fixed at 444.4, 444.7, 445.3 and 445.7 eV, respectively [26]. Figure 4(b) summarizes the relative peak area ratios of the various components. It can be clearly observed that the InP component was effectively enhanced and the oxide components were effectively reduced after the insertion of Al_2O_3, which could be attributed to the inserted Al_2O_3 suppressing substrate oxidation and preventing the diffusion of substrate elements.

Figure 5(a) shows the gate leakage current density (*J*) versus electric field (*E*) characteristics of the InP MOSCAPs with a single 6 nm HfO_2 dielectric, 4 nm HfO_2/1 nm Al_2O_3 and 4 nm HfO_2/2 nm Al_2O_3 gate stacks under positive gate bias with electrons injected from the InP substrate at room temperature. Since these InP MOSCAPs have different thicknesses and may therefore have different leakage currents, the gate electric field instead of the gate bias was used for comparison. Compared with the InP MOSCAP with a single 6 nm HfO_2 dielectric, the capacitor with a 4 nm HfO_2/2 nm Al_2O_3 gate stack exhibited a much lower gate leakage current. This could be attributed to the larger bandgap of Al_2O_3 than that of HfO_2, which resulted in an increased band offset at the InP surface in figure 1(b). Besides, with decreasing thickness of the Al_2O_3 passivation layer, the gate leakage current was slightly

Table 1. The main parameters for the InP MOSCAPs in this work.

Parameter	6 nm HfO_2	4 nm HfO_2/ 1 nm Al_2O_3	4 nm HfO_2/ 2 nm Al_2O_3
Frequency dispersion (%)	69.0	15.5	7.7
D_{it} ($\times 10^{11}$ cm^{-2} eV^{-1})	4.4	4.0	3.8
V_{FB} (V)	0.50	0.18	0.26
J_g @ 1 MV cm^{-1} (mA cm^{-2})	7.9	1.0	0.62
Conduction mechanism	F-P	F-P to F-N	F-P to F-N

increased due to the reduced thickness but still lower than that of the capacitor with a single HfO_2 dielectric. To further investigate the mechanism of the reduced leakage current after the insertion of the Al_2O_3 passivation layer, current fitting for the InP MOSCAPs with a single 6 nm HfO_2 dielectric, 4 nm HfO_2/1 nm Al_2O_3 and 4 nm HfO_2/2 nm Al_2O_3 was performed, as shown in figure 4(b). From the fitting results, for the capacitor with a single HfO_2 dielectric, the leakage current was dominated by the trap-assisted Frenkle–Poole (F-P) emission mechanism. However, for the capacitors with stacked dielectrics incorporating Al_2O_3 passivation, the leakage current followed the F-P conduction mechanism in the low-E region but the Fowler–Nordheim (F-N) tunneling mechanism in the high-E region, as shown in the inset of figure 5(b). With a positive gate bias applied, the leakage current may mainly be influenced by trap or defect related conduction at the InP interface, where the traps or defects may be induced by the diffusion of substrate elements [16, 28, 31]. After inserting the Al_2O_3 passivation layer between HfO_2 and the InP substrate, substrate diffusion could be effectively suppressed, with the result that the leakage mechanism changed from F-P conduction in the low-E region to F-N conduction in the high-E region due to the improved interface quality. These results were consistent with the D_{it} distribution discussed above.

Table 1 summarizes the main parameters of the InP MOSCAPs with a single 6 nm HfO_2 dielectric, 4 nm HfO_2/1 nm Al_2O_3 and 4 nm HfO_2/2 nm Al_2O_3 found in this work. It can be observed the V_{FB} was reduced after inserting an Al_2O_3 passivation layer, which could be ascribed to the improved interface due to suppression of substrate oxidation by the insertion of Al_2O_3. More importantly, it can also be seen that the InP MOSCAP with a stacked 4 nm HfO_2/2 nm Al_2O_3 dielectric achieved the lowest D_{it} of $\sim 3.8 \times 10^{11}$ cm^{-2}eV^{-1}, which was comparable to that of the previously reported InP MOSCAPs ($\sim 2 \times 10^{11}$–1×10^{13} cm^{-2} eV^{-1}) [14–16, 26].

4. Conclusion

This work investigated the effect of insertion of an Al_2O_3 passivation layer for atomic layer deposited HfO_2 on an InP substrate. By inserting Al_2O_3 between HfO_2 and the InP substrate, the frequency dispersion, leakage current and D_{it} were effectively improved, which could be ascribed to the Al_2O_3 passivation layer with a large bandgap that suppressed substrate oxidation and elemental diffusion. On decreasing the thickness of the Al_2O_3 layer from 2 to 1 nm, the characteristics including frequency dispersion and D_{it} were slightly degraded due to the fact that diffusion from the substrate was not effectively suppressed and substrate oxidation may be induced after PDA. This approach of proper selection of the passivation layer provides a solution for improving the interface quality for InP semiconductors, and has great potential for future applications of InP devices with low power consumption and high frequency.

Data availability statement

The data that support the findings of this study are available upon reasonable request from the authors.

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References

[1] Rezazadeh V G, Bothe K M, Afshar A, Cadien K C and Barlage D W 2016 Defect characterization of PEALD high-*k* ZrO_2 films fabricated on III–V materials *IEEE Trans. Semicond. Manuf.* **29** 355–62
[2] Smit M *et al* 2014 An introduction to InP-based generic integration technology *Semicond. Sci. Technol.* **29** 083001
[3] Walukiewicz W, Lagowski J, Jastrzebski L, Rava P, Lichtensteiger M, Gatos C H and Gatos H C 1980 Electron mobility and free-carrier absorption in InP; determination of the compensation ratio *J. Appl. Phys.* **51** 2659–68
[4] Zhao H, Shahrjerdi D, Zhu F, Kim H-S, Ok I, Zhang M, Yum J H, Banerjee S K and Lee J C 2008 Inversion-type indium phosphide metal–oxide–semiconductor field-effect transistors with equivalent oxide thickness of 12 Å using stacked $HfAlO_x$/HfO_2 gate dielectric *Appl. Phys. Lett.* **92** 253506
[5] Herbert R E, Hwang Y and Stemmer S 2010 Comparison of methods to quantify interface trap densities at dielectric/III–V semiconductor interfaces *J. Appl. Phys.* **108** 124101
[6] He G, Chen X S and Sun Z Q 2013 Interface engineering and chemistry of Hf-based high-*k* dielectrics on III–V substrates *Surf. Sci. Rep.* **68** 68–107
[7] Gao J, He G, Xiao D Q, Jin P, Jiang S S, Lia W D, Liang S and Zhu L 2017 Passivation of Ge surface treated with trimethylaluminum and investigation of electrical properties of HfTiO/Ge gate stacks *J. Mater. Sci. Technol.* **33** 901–6
[8] Yang Z, Yang J Z, Huang Y, Zhang K and Hao Y 2014 Effect of alumina thickness on Al_2O_3/InP interface with post deposition annealing in oxygen ambient *Chin. Phys.* B **23** 077305
[9] Suzuki R *et al* 2012 1-nm-capacitance-equivalent-thickness HfO_2/Al_2O_3/InGaAs metal-oxide-semiconductor structure with low interface trap density and low gate leakage current density *Appl. Phys. Lett.* **100** 132906
[10] Choi J H, Mao Y and Chang J P 2011 Development of hafnium based high-κ materials—a review *Mater. Sci. Eng.* R **72** 97–136

[11] Vavasour O J, Jefferies R, Walker M, Roberts J W, Meakin N R, Gammon P M, Chalker P R and Ashley T 2019 Effect of HCl cleaning on InSb–Al_2O_3 MOS capacitors *Semicond. Sci. Technol.* **34** 035032
[12] An C H, Byun Y C, Lee M S and Kim H 2011 Thermal stabilities of ALD-HfO_2 films on HF- and $(NH_4)_2S$-cleaned InP *ECS J. Electrochem. Soc.* **158** G242–45
[13] Haimoto T, Hoshii T, Nakagawa S, Takenaka M and Takagia S 2010 Fabrication and characterization of metal-insulator-semiconductor structures by direct nitridation of InP surfaces *Appl. Phys. Lett.* **96** 012107
[14] Wang S K, Sun B, Cao M M, Chang H D, Su Y Y, Li H O and Liu H G 2017 Modification of Al_2O_3/InP interfaces using sulfur and nitrogen passivations *J. Appl. Phys.* **121** 184104
[15] Lee J S, Ahn T Y and Kim D 2019 Facile process for surface passivation using $(NH_4)_2S$ for the InP MOS capacitor with ALD Al_2O_3 *Materials* **12** 3917
[16] Mahata C, Oh I K, Yoon C M, Lee C W, Seo J, Algadi H, Sheen M H, Kim Y W, Kima H and Lee T 2015 The impact of atomic layer deposited SiO_2 passivation for high-*k* $Ta_{1-x}Zr_xO$ on the InP substrate *J. Mater. Chem.* C **3** 10293–301
[17] Lin C A *et al* 2012 InAs MOS devices passivated with molecular beam epitaxy-grown Gd_2O_3 dielectrics *J. Vac. Sci. Technol.* B **30** 02B118
[18] Cheng C H, Hsu H H and Chou K I 2015 TiO_2-based indium phosphide metal-oxide-semiconductor capacitor with high capacitance density *J. Nanosci. Nanotechnol.* **15** 2810–3
[19] Kobayashi H, Imamura K, Fukayama K I, Im S S, Maida O, Kim Y B, Kim H C and Choi D K 2008 Complete prevention of reaction at HfO_2/Si interfaces by 1 nm silicon nitride layer *Surf. Sci.* **602** 1948–53
[20] Greene A, Madisetti S, Nagaiah P, Yakimov M, Tokranov V, Moore R and Oktyabrsk S 2012 Improvement of the GaSb/Al_2O_3interface using a thin InAs surface layer *Solid-State Electron.* **28** 56–61
[21] Aokia T, Fukuhara N, Osada T, Sazawa H, Hata M and Inoue T 2015 Electrical properties of GaAs metal–oxide–semiconductor structure comprising Al_2O_3 gate oxide and AlN passivation layer fabricated *in situ* using a metal–organic vapor deposition/atomic layer deposition hybrid system *AIP Adv.* **5** 087149
[22] Dong H *et al* 2018 C-V and J-V investigation of HfO_2/Al_2O_3 bilayer dielectrics MOSCAPs on (100) β-Ga_2O_3 *AIP Adv.* **8** 065215
[23] O'Mahony A *et al* 2010 Structural and electrical analysis of thin interface control layers of MgO or Al_2O_3 deposited by atomic layer deposition and incorporated at the high-k/III–V interface of $MO_2/In_xGa_{1-x}As$ (M = Hf|Zr, x = 0|0.53) gate stacks *ECS Trans.* **33** 69–82
[24] Mahata C, Byun Y C, An C H, Choi S, An Y and Kim H 2013 Comparative study of atomic-layer-deposited stacked (HfO_2/Al_2O_3) and nanolaminated ($HfAlO_x$) dielectrics on $In_{0.53}Ga_{0.47}As$ *ACS Appl. Mater. Interfaces* **5** 4195–201
[25] Kang Y S, Kim D K, Jeong K S, Cho M H, Kim C Y, Chung K B, Kim H and Kim D C 2013 Structural evolution and the control of defects in atomic layer deposited HfO_2–Al_2O_3 stacked films on GaAs *ACS Appl. Mater. Interfaces* **5** 1982–9
[26] Kang H K, Kang Y S, Kim D K, Baik M, Song J D, An Y, Kim H and Cho M H 2017 Al_2O_3 passivation effect in $HfO_2 \cdot Al_2O_3$ laminate structures grown on InP substrates *ACS Appl. Mater. Interfaces* **9** 17526–35
[27] Suh D C, Cho Y D, Kim S W, Ko D H, Lee Y, Cho M H and Oh J 2010 Improved thermal stability of $Al_2O_3/HfO_2/Al_2O_3$ high-k gate dielectric stack on GaAs *Appl. Phys. Lett.* **96** 142112
[28] Baik M, Kang H K, Kang Y S, Jeong K S, An Y, Choi S, Kim H, Song J D and Cho M H 2017 Electrical properties and thermal stability in stack structure of HfO_2/Al_2O_3/InSb by atomic layer deposition *Sci. Rep.* **7** 11337
[29] Suh D C, Cho Y D, Ko D H, Lee Y, Chung K B and Cho M H 2010 Effects of interface Al_2O_3 passivation layer for high-k HfO_2 on GaAs *Electrochem. Solid-State Lett.* **14** H63–5
[30] Qiao L S, He G, Hao L, Lu J Y, Gao Q, Zhang M and Fang Z B 2021 Interface optimization of passivated Er_2O_3/Al_2O_3/InP MOS capacitors and modulation of leakage current conduction mechanism *IEEE Trans. Electron Devices* **68** 2899–905
[31] An C H, Byun Y C, Cho M H and Kim H 2012 Thermal instability of HfO_2 on InP structure with ultrathin Al_2O_3 interface passivation layer *Phys. Status Solidi* **6** 247–9
[32] Wang Y Z, Zhao H, Chen Y T, Xue F, Zhou F and Lee J 2010 Atomic-layer-deposition HfO_2-based InP n-channel metal-oxide-semiconductor field effect transistor using different thicknesses of Al_2O_3 as interfacial passivation layer *ECS Trans.* **33** 487–93
[33] Hiraiwa A, Matsumura D and Kawarada H 2016 Effect of atomic layer deposition temperature on current conduction in Al_2O_3 films formed using H_2O oxidant *J. Appl. Phys.* **120** 084504
[34] Zheng W J, Bowen K H, Li J, Daọbkowska I and Gutowski M 2005 Electronic structure differences in ZrO_2 vs HfO_2 *J. Phys. Chem.* A **109** 11521–5
[35] Pham T T, Rouger N, Masante C, Chicot G, Udrea F, Eon D, Gheeraert E and Pernot J 2017 Deep depletion concept for diamond MOSFET *Appl. Phys. Lett.* **111** 173503
[36] Arora N 1993 *MOSFET Models for VLSI Circuit Simulation* (Berlin: Springer)
[37] Sonnet A M, Hinkle C L, Heh D, Bersuker G and Vogel E M 2010 Impact of semiconductor and interface-state capacitance on metal/high-k/GaAs capacitance–voltage characteristics *IEEE Trans. Electron Devices* **57** 2599–606
[38] Hasegawa H and Sawada T 1980 Electrical modeling of compound semiconductor interface for FET device assessment *IEEE Trans. Electron Devices* **27** 1055–61
[39] Sze S M and Ng K K 2006 *Physics of Semiconductor Devices* (New York: Wiley)