Impact of Random Interface Traps Fluctuation on Device Variation of Oxide-Semiconductor Ferroelectric Field-Effect Transistor Memories

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***Abstract*— In this letter, we systematically investigate the impact of randomly distributed ferroelectric/interlayer (FE/IL) and interlayer/oxide-semiconductor (IL/OS) interface traps, both individually and in combination, on the variability of oxide-semiconductor ferroelectric field-effect transistor (OS-FeFET) memory devices. Our study demonstrates that: 1) as the density of IL/OS interface traps ($N_{IL/OS}$) increases, the memory window (MW) exhibits significant fluctuation with a larger σ_{MW}, resulting in the degradation of μ_{MW}; 2) MW is impacted by the density of FE/IL interface traps ($N_{FE/IL}$) by modifying the electric field in FE and IL layers, consequently leading to a substantial μ_{MW} but no obvious change in σ_{MW}; 3) when considering the combined impact of both types of traps, the impact of FE/IL interface traps on increasing μ_{MW} is suppressed with an increased $N_{IL/OS}$. However, it is crucial to note that although the larger $N_{IL/OS}$ dominates the overall MW fluctuation, the fluctuation caused by $N_{FE/IL}$ cannot be disregarded especially with smaller $N_{IL/OS}$. These findings provide valuable insights into the understanding of interface trap effects on the device variation of OS-FeFET memories.**

***Index Terms*— FeFET, oxide semiconductor, interface traps, memory window, variation.**

I. Introduction

HAFNIA-BASED ferroelectric field-effect transistors (FeFETs) have garnered significant attention for their advantages in non-volatile memory (NVM) applications, including good scalability, compatibility with CMOS, high density, fast read/write speed, and low power consumption [1], [2], [3], [4], [5], [6]. A high-density vertical-channel FeFET structure using poly-Si channel has been successfully demonstrated for 3D integration applications [7], [8]. However, there are still challenges, such as low mobilty of poly-Si channel, low-k interfacial layer formation, and high thermal budget [9]. Recently, oxide semiconductor, such as IGZO, has been proposed to replace conventional poly-Si channel as a suitable channel material for FeFETs due to its high mobility as an amorphous material, no low-k interficial layer, low thermal budget, and junctionless FET operation [10], [11]. To date, most of the reported OS-FeFETs are bottom-gate structures with channel-last process, which avoids the undesirable low-k IL formation due to low thermal budget. However, the oversized gate design results in extra parasitic gate-channel-S/D overlap capacitance, and the non-self-aligned gate process can cause the current drive loss [12]. Therefore, it is necessary to develop low-thermal-budget top-gate OS-FeFETs to leverage self-aligned gate-S/D patterning capability for easing aggressive transistor feature size and circuit density scaling. These top-gate structures with channel-first process, which are commonly used in Si-based FeFETs, may result in uncontrollable FE/OS interface quality due to the process conditions of film deposition and annealing [13]. Thus, intentional preparation of a high-quality IL between FE and OS layer is needed, which is applied even in bottom-gate structures for performance improvements [14], [15]. For conventional FeFETs with Si channel, it has been reported that the trap charges at either FE/IL or IL/Si interface in the gate stack affect the memory characteristics, such as MW, endurance, and retention [16], [17], [18], [19], [20]. Nevertheless, the analysis on the interface traps has been rarely studied for OS-FeFETs with the IL. Since the interface traps are randomly distributed, the interface trap induced variability is expected to be of great importance for the devices. Therefore, in this work, with the aid of TCAD simulation, we investigate the IGZO-channel FeFET device variation induced by random spatial traps fluctuation from FE/IL and IL/OS interface individually and in combination.

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II. Simulation Methodology

A schematic of the OS-FeFET structure with HZO and IGZO as the FE and OS channel layer, respectively, along with an illustration of randomly distributed interface traps, is presented in Fig. 1(a). To describe FE multi-domain, the Preisach model is employed in simulation [21], [22]. Fig. 1(b) shows the calibration of the FE parameters with the experimental P-V data of a FE capacitor [23]. Here, the remnant polarization (P_r) and saturation polarization (P_s) are 20 and 23 $\mu C/cm^2$, respectively, corresponding to a coercive field (E_c) of 1.5 MV/cm. A good agreement is achieved between the simulated and reported experimental P-V data. Furthermore, IGZO material with a bandgap of 3.2 eV, an electron affinity energy of 4.16 eV, and a dielectric permittivity of 10 was implemented by density of state (DOS) model in simulation.

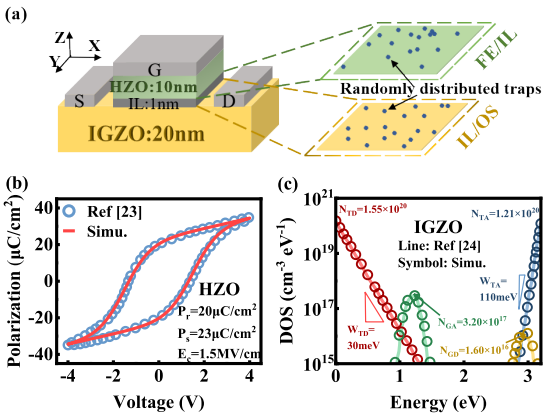

Fig. 1. (a) Schematic structure of the OS-FeFET with 10 nm HZO and 20 nm IGZO, along with randomly distributed interface traps, (b) FE parameter calibration with the experimental P-V data [23], and (c) the DOS of IGZO material calibrated from the reported data [24].

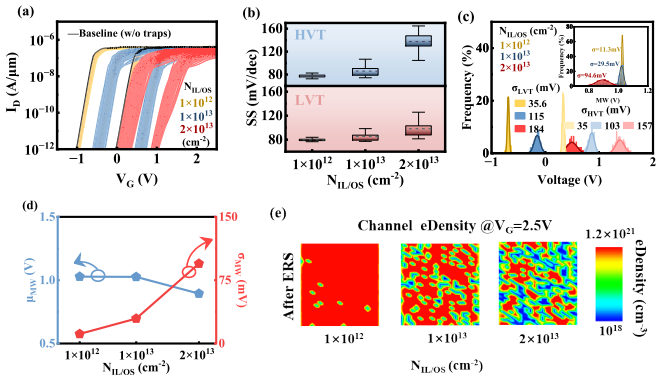

Fig. 2. (a) Dispersive I_D-V_G curves for OS-FeFETs with different $N_{IL/OS}$, (b) SS at HVT and LVT states as a function of $N_{IL/OS}$, (c) LVT/HVT distributions (inset: MW distributions) extracted from I_D-V_G curves with different $N_{IL/OS}$, (d) extracted μ_{MW} and σ_{MW} as a function of $N_{IL/OS}$, and (e) channel electron density distributions at $V_G = 2.5$ V after ERS with different $N_{IL/OS}$.

Fig. 1(c) shows the DOS of IGZO material, which is well calibrated from the reported data [24]. Here, DOS parameters include valance and conduction band tail states at band edges (N_{TD} and N_{TA}), tail state slope (W_{TD} and W_{TA}), acceptor-like and donor-like states with Gaussian distributions (N_{GA} and N_{GD}) along with their full width at half maximums (W_{GA} and W_{GD}). The gate length and width of the devices are 40 and 40 nm, respectively. For memory operation, separate erase state (HVT state) and program state (LVT state) are set by using square gate pulses (100 ns) with amplitude of -5 and 5 V, respectively. Then a bias voltage of 0.05 V is applied to the drain and the I_D-V_G curve of the device is obtained by scanning the gate bias voltage.

In this work, we have considered the fixed (acceptor) traps at the FE/IL and IL/OS interface, taking into account that IGZO is an n-type semiconductor. The density of the related traps is within reasonable ranges [17], [18], [19]. Both traps are randomly distributed and do not influence each other. To better describe the interface trap induced device variation, we simulate three separate groups (100 devices each) of OS-FeFET devices.

III. Results and Discussion

A. w/o FE/IL Interface Traps, w/ IL/OS Interface Traps

Fig. 2(a) shows the transfer I_D-V_G curve dispersions for the OS-FeFETs with different $N_{IL/OS}$. The black curves are ideal for the baseline device without traps. It can be found that the presence of IL/OS interface traps results in significant fluctuation for both HVT and LVT states. With the $N_{IL/OS}$ increasing, both HVT and LVT shift in positive direction and their fluctuation becomes larger. Meanwhile, the corresponding subthreshold swing (SS) degrades, as summarized in Fig. 2(b), indicating the impact of IL/OS interface traps. Fig. 2(c) presents the LVT and HVT distributions with the MW distributions in the inset, which are extracted from I_D-V_G curves with different $N_{IL/OS}$. Fig. 2(d) shows the extracted mean (μ_{MW}) and standard deviation (σ_{MW}) for the MW as a function of $N_{IL/OS}$. It can be found that as the $N_{IL/OS}$ increases, the LVT state is more significantly affected than the HVT state and the MW is degraded. The MW degradation can be ascribed to the screened FE polarization by IL/OS interface traps [17]. After program operation with the positive gate pulse, many electrons are induced near the channel interface at the LVT state. These electrons can be easily screened away from the channel interface by the acceptor-type IL/OS interface traps [25]. It indicates that the $N_{IL/OS}$ has pronounced impact on the LVT state than the HVT state. The larger $N_{IL/OS}$ is, the more severe the impact is. Thus, as the $N_{IL/OS}$ increases, the LVT state exhibits a larger distribution as compared with the HVT state, resulting in the obvious asymmetry in the LVT and HVT variability under the $N_{IL/OS}$ of 2×10^{13} cm^{-2}. To explain the spread of MW distributions (larger σ_{MW}) with the $N_{IL/OS}$ increasing, the channel electron density distributions at $V_G = 2.5$ V after erase with different $N_{IL/OS}$ is illustrated in Fig. 2(e). The nonuniform distribution of channel electron density is obviously observed for the larger $N_{IL/OS}$ case, which is in good agreement with larger σ_{MW}.

B. w/ FE/IL Interface Traps, w/o IL/OS Interface Traps

Fig. 3(a) and (b) shows the dispersive I_D-V_G curves and extracted MW distributions, respectively, for the OS-FeFETs with different $N_{FE/IL}$. Fig. 3(c) illustrates the extracted μ_{MW} and σ_{MW} as a function of $N_{FE/IL}$. As the $N_{FE/IL}$ increases, the μ_{MW} becomes larger while the σ_{MW} exhibits only a slight increase. Additionally, the SS is almost not affected. These phenomenon are quite different from that caused by $N_{IL/OS}$. The increased MW with higher $N_{FE/IL}$ can be attributed to the acceptor-type FE/IL interface trap-assisted polarization enhancement [26]. With the positive gate voltage applied (LVT state), the trapped electrons at the FE/IL interface screen the electric flux from FE polarization, resulting in the reduction of IL electric field (E_{IL}). Fig. 3(d) shows the change of the energy band diagram for the devices with and without FE/IL interface traps at $V_G = 5$ V. It can be seen that the energy band becomes higher at FE/IL interface with FE/IL interface traps as compared to that without traps, indicating the strengthened FE electric field (E_{FE}) and weakened E_{IL} simultaneously. Thus, the increased $N_{FE/IL}$ could lead to an increase of E_{FE}, assisting the polarization switching. However, with the negative gate voltage applied (HVT state), there

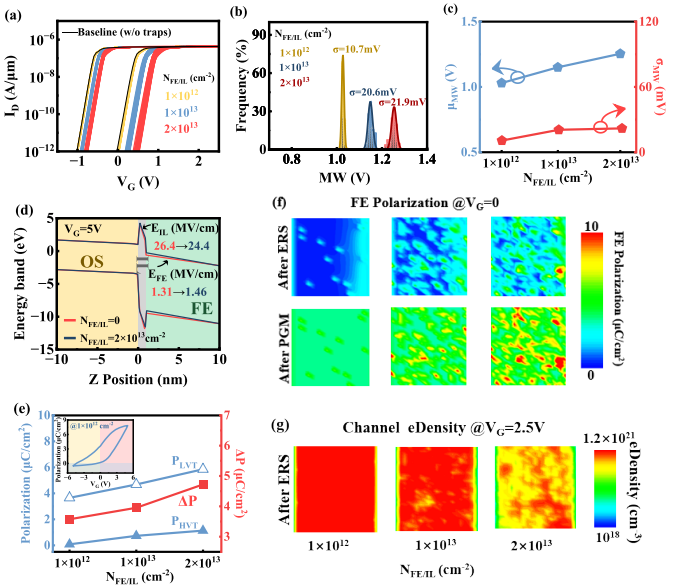

Fig. 3. (a) Dispersive I_D–V_G curves for OS-FeFETs with different $N_{FE/IL}$, (b) MW distributions extracted from I_D-V_G curves with different $N_{FE/IL}$, (c) extracted μ_{MW}, σ_{MW} as a function of $N_{FE/IL}$, (d) energy band diagram for the devices with and without FE/IL interface traps at V_G = 5 V, (e) P_{LVT}, P_{HVT}, ΔP as a function of $N_{FE/IL}$ (inset: P-V curve for $N_{FE/IL} = 1 \times 10^{12}$ cm^{-2}), (f) FE polarization distributions at V_G = 0 V after program and erase, and (g) channel electron density distributions at V_G = 2.5 V after ERS with different $N_{FE/IL}$.

are few trapped holes to assist the polarization switching [27]. This can be confirmed by the asymmetric polarization characteristics in Fig. 3(e), where a large polarization (P_{LVT}) can be induced during program but only a small polarization (P_{HVT}) can be induced during erase. The increase of the $N_{FE/IL}$ leads to larger polarization, which is consistent with the FE polarization distributions in Fig. 3(f). Moreover, since the FE/IL interface traps can also induce positive shift for both HVT and LVT states, the MW is determined by both the polarization enhancement (particularly at the LVT state) and trap-induced V_T shift. By considering these, as compared to the HVT, the LVT shifts slightly because the polarization enhancement and trap-induced V_T shifts in the opposite direction. Due to the random distribution of FE/IL interface traps, uneven polarization of the FE layer is induced, which further affects the potential across the gate stack, resulting in the channel electron density fluctuation. Fig. 3(g) shows the channel electron density distributions at V_G = 2.5 V after erase with different $N_{FE/IL}$, which remains relatively uniform, confirming the slight σ_{MW} variation. This uniform channel electron density distribution could be ascribed to the IL layer, which suppresses potential fluctuation and makes the channel electron density become relatively homogeneous.

C. With FE/IL Interface Traps and IL/OS Interface Traps

To reveal the combined impact of both FE/IL and IL/OS interface traps, we analyze the impact of $N_{IL/OS}$ (or $N_{FE/IL}$) with different densities at different constant $N_{FE/IL}$ (or $N_{IL/OS}$). Fig. 4(a) presents the simultaneous impact of both types of interface traps on μ_{MW}. It can be observed that as the $N_{FE/IL}$ increases, the μ_{MW} gradually increases. This effect

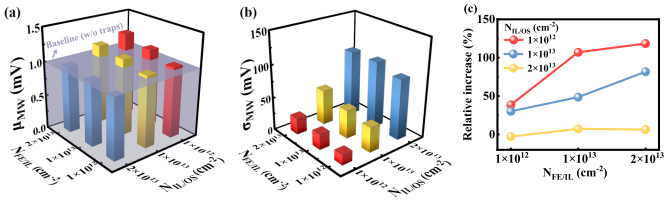

Fig. 4. Simultaneous impact of both FE/IL and IL/OS interface traps on (a) μ_{MW} and (b) σ_{MW}, and (c) the relative increase in σ_{MW} as a function of $N_{FE/IL}$ at constant $N_{IL/OS}$.

is correlated with $N_{IL/OS}$ and can be suppressed with the increase of the $N_{IL/OS}$, which could be due to their individual impact with opposite behavior in MW. Fig. 4(b) illustrates the simultaneous impact of both types of interface traps on σ_{MW}. The most noticeable trend is that the MW fluctuation greatly increases with the increase in $N_{IL/OS}$ at a certain $N_{FE/IL}$. However, the increased $N_{FE/IL}$ leads to a relatively slow increase in MW fluctuation at a certain $N_{IL/OS}$. This indicates that the $N_{IL/OS}$ dominates the overall MW fluctuation. To better evaluate the MW variability with the combined impact of the $N_{FE/IL}$ and $N_{IL/OS}$, the relative increase in σ_{MW} as a function of $N_{FE/IL}$ at constant $N_{IL/OS}$ is plotted in Fig. 4(c). Here, the relative increase refers to the ratio of the σ_{MW} value of the absolute increase to the value of the σ_{MW} at $N_{FE/IL} = 0$. It can be observed that when $N_{IL/OS}$ exceeds a critical value (1×10^{13} cm^{-2}), the increment in fluctuation caused by $N_{FE/IL}$ is relatively small. It indicates that the MW fluctuation is mainly dominated by IL/OS interface traps when $N_{IL/OS}$ is large enough. When $N_{IL/OS}$ is below the critical value, the increment in MW fluctuation enhances with the increase in $N_{FE/IL}$. This means that the MW fluctuation caused by FE/IL interface traps cannot be ignored with small $N_{IL/OS}$. Therefore, in device variation analysis, the impact of both FE/IL and IL/OS interface traps should be considered comprehensively, which is essential for OS-FeFET devices.

IV. Conclusion

The impact of randomly distributed FE/IL and IL/OS interface traps on the device variation of OS-FeFET memories has been comprehensively investigated by TCAD simulation individually and in combination. Our study demonstrates that higher $N_{IL/OS}$ leads to a noticeable decrease in MW and a great increase in MW fluctuation, together with degraded SS. While higher $N_{FE/IL}$ causes an improved MW and a slightly increase in MW fluctuation. Taking both FE/IL and IL/OS interface traps into consideration, the MW enhancement effect caused by FE/IL interface traps is further weakened with increasing IL/OS interface traps. There exists a critical $N_{IL/OS}$ at which IL/OS interface traps dominate the overall MW fluctuation above this trap density. Below this critical value, the MW variability caused by both IL/OS and FE/IL interface traps cannot be ignored. In addition, it should be pointed out that OS-FeFETs with nearly-zero low-k interfacial layer between FE and OS layers has also been reported [9], [10], [11], which has not been addressed in this work and needed further investigation on the impact of FE/OS interface trap fluctuation. The present results in this letter may provide a physical insight and trigger more comprehensive analyses on the impact of interface traps in OS-FeFET memories.

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