Semiconductor Science and Technology

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IOP Publishing Semiconductor Science and Technology
Semicond. Sci. Technol. **38** (2023) 045003 (5pp) https://doi.org/10.1088/1361-6641/acb8a7

The impact of charges at the dielectric/channel interface on performance degradation in negative capacitance ferroelectric FETs

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Received 21 September 2022, revised 7 December 2022
Accepted for publication 3 February 2023
Published 23 February 2023

Abstract

In this study, the impact of interfacial charges including fixed charges and acceptor-type traps between the dielectric and the channel in negative capacitance ferroelectric FETs (FeFETs) is investigated by simulation based on the Landau–Khalatnikov model. The results reveal the separate impact of the fixed charges and acceptor-type traps on device performance degradation, respectively, including the subthreshold swing (*SS*), switching current (I_{on} and I_{off}) and threshold voltage (V_T). On this basis, the combined impact of interfacial charges with the fixed charges and acceptor-type traps co-existing equally is further explored. Our findings indicate that the fixed charges play a key role in the V_T and I_{off}, while the acceptor-type traps predominate in the *SS* and I_{on}. This study helps to understand the degradation mechanism of FeFETs and extend the device end-of-lifetime.

Keywords: ferroelectric, negative capacitance, interfacial charges, subthreshold swing

(Some figures may appear in colour only in the online journal)

1. Introduction

Integrated circuits urgently need to develop new types of low-power microelectronic devices as Moore's law gradually reaches its physical limits. Ferroelectric FETs (FeFETs) can achieve gate voltage amplification through the negative capacitance (NC) effect of ferroelectric materials, which achieves a subthreshold swing (*SS*) below the fundamental Boltzmann limit of 60 mV dec^{-1} at room temperature [1–3]. With the discovery of ferroelectricity in doped hafnia, hafnia-based FeFETs have become one of the most promising candidates for logic and memory devices. Recently, numerous investigations have been carried out on the NC effect in FeFETs, including various aspects such as capacitance matching [4–7], device parameters [8–10] and manufacturing processes [11–13]. For a transistor, the impact of traps/charges at the interface can degrade the device performance in terms of threshold voltage (V_T) shift and *SS* degradation, thus causing certain reliability issues [14–19]. Many studies, by considering the traps at the dielectric (DE)/channel interface, have been well established in MOSFETs with traditional DEs [20–23]. However, the interface issue is still not fully understood in FeFETs with the metal-FE-insulator-silicon (MFIS) structure by incorporating

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a high-permittivity FE layer. Most studies so far have analyzed the trap/charge behavior at the FE/DE interface [12, 13, 24]. The DE/channel interface is equally of great importance but has not been studied in detail. At the DE/channel hetero-interface, there may be different types of interfacial charges. One is the fixed charges originating from the defects that are either always occupied or not occupied by the electrons. The other is the acceptor-type traps, where the number of captured charges is affected by the gate voltage and some can be transformed into residual charges due to the bias temperature instability (BTI) effect [23, 24]. However, some studies have only analyzed the impact of a single type of charges at the DE/channel interface on certain device characteristics [25, 26], which is not comprehensive enough and can be further studied. Although the combined impact of charges at different interfaces in FeFETs has been studied [27], the interaction between different types of charges at the same interface on device performance has not been investigated. Therefore, the combined impact of interfacial charges, including the fixed charges and acceptor-like traps at the DE/channel interface, needs further detailed investigation.

In this work, we consider both the fixed charges and acceptor-type traps at the DE/channel interface in an *n*-type MFIS hafnia-based FeFET using the Landau–Khalatnikov (LK) model. We analyzed the device performance for the case where the traps were not fully recovered. The impacts of the fixed charges and acceptor-type traps on the device performance, including V_T, *SS*, I_{on} and I_{off}, were studied separately and compared. On this basis, we further investigated the combined impact of both charges on the device performance. The obtained results in this work could provide a solution to understand the physical mechanism of the device performance degradation in FeFETs.

2. Device structure and simulation model

Figure 1(a) shows the schematic structure of the simulated FeFET device, where Si, HfZrO and SiO_2 are chosen as the channel material, FE and DE insulators, respectively. The fixed charges and acceptor-type traps are assumed at the DE/channel interface. Figure 1(b) depicts the equivalent circuit of the FeFET by considering the charges at the DE/channel hetero-interface. The ferroelectric model is established based on the LK equation, which is given by [29]:

$$-\rho\frac{\mathrm{d}P}{\mathrm{d}t} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 - E_F \qquad (1)$$

where α, β and γ are LK parameters, ρ is the viscosity that represents a kinetic coefficient associated with the polarization switching, P is the polarization and E_F is the local electric field in the FE layer. The LK model has been widely used in HfO_2-based ferroelectric materials, and can exhibit the properties of HfO_2-based ferroelectric materials well [1–5, 25–27].

We made the experiment-based calibration for the LK model by fitting it with experimental data [28], as shown in figure 2(a). The simulated *S*-curve in the *P*–*V* characteristic

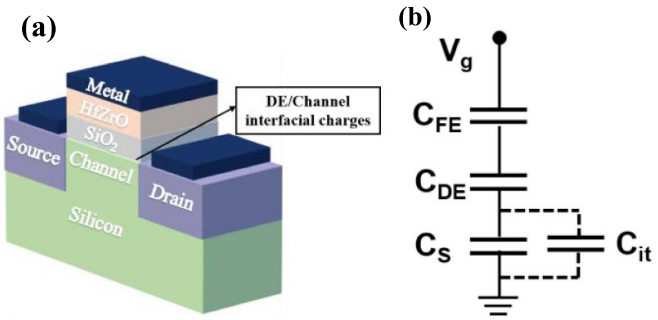

Figure 1. (a) The schematic structure and (b) equivalent circuit of the FeFET device.

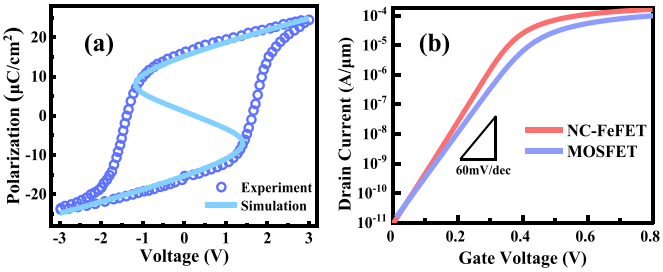

Figure 2. (a) *P*–*V* calibration for the experimental data [28], and (b) I_d–V_g curves at $V_d = 0.05$ V for the NC-FeFET and baseline MOSFET.

Table 1. The main simulation parameters.

Simulation parameters	Value
LK parameter α	-8.2×10^{10} cm/F
LK parameter β	4.2×10^{12} cm^5/(F·C^2)
LK parameter γ	5×10^{29} cm^9/(F·C^4)
Relative dielectric constant for SiO_2	3.9
Relative dielectric constant for HZO	25
S/D doping concentration	10^{19} cm^{-3}
Channel doping concentration	5×10^{17} cm^{-3}
Gate work function	4.43 eV
Gate length	100 nm
FE thickness	8 nm
Oxide thickness	1 nm

presents a reasonable match with the experimental data. The LK parameters of ferroelectric materials extracted from the experimental data are shown in table 1.

Figure 2(b) shows the simulated I_d–V_g characteristics of the FeFET with the MFIS structure based on the LK model and the baseline MOSFET without the FE layer. The corresponding simulation parameters are shown in table 1. The obtained minimum *SS* (SS_{min}) of the FeFET and baseline MOSFET were 56 and 66 mV dec^{-1}, respectively, as a result of the incorporation of the NC effect. These results are simulated by solving Poisson's equation, the drift-diffusion equation and the LK equation self-consistently at each mesh point of the device.

For the consideration of the interfacial charges between the DE and the channel, the simulation includes the fixed charges

and acceptor-type traps, which are randomly distributed and commonly considered in n-type FeFET devices [26, 27, 30]. It is worth noting that the charge concentrations used in this work are consistent with the relevant existing studies [25, 27]. The model also takes into account a variety of physical mechanisms, such as carrier recombination and generation, mobility degradation induced by impurity scattering and carrier–carrier scattering, quantum mechanical effects, and velocity saturation of high field effects.

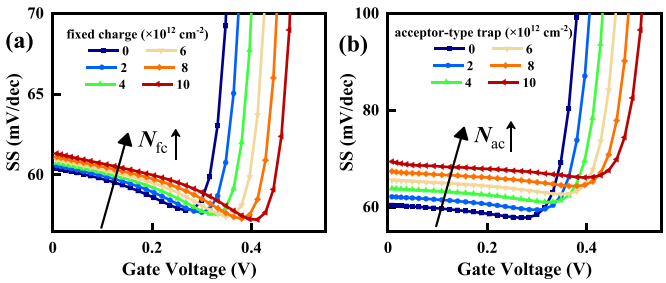

Figure 3. *SS* as a function of V_g at different (a) N_{fc} and (b) N_{ac}.

3. Results and discussion

Figures 3(a) and (b) show the impact of the fixed charges and acceptor-type traps on the *SS*, respectively. The deterioration of the *SS* can be observed as the concentration of the fixed charges and acceptor-type traps (N_{fc} and N_{ac}) increases. However, the impact of the acceptor-type traps on the *SS* still differs significantly from that of the fixed charges. At low V_g, the *SS* variation that considers the N_{ac} is substantially larger in magnitude than that which considers the N_{fc}, which could be attributed to the fact that the concentration of charges captured by the acceptor-type traps increases with the V_g increase, resulting in an additional change in charge. Thus, it reduces the ability of the gate voltage to control the channel [27]. Similarly, it is clearly observed that the SS_{min} increases with the N_{ac} increase, which could be ascribed to the larger change in charge caused by the increase of the N_{ac}.

Besides the *SS*, the I_{on}, I_{off} and V_T are also important figures of merit for the device. The I_{on} and I_{off} are extracted at the $V_g = 0.8$ and 0 V, respectively, and the V_T is extracted using the constant current method. Figures 4(a) and (b) show the impact of the fixed charges and acceptor-type traps individually on the switching current including I_{on} and I_{off}, respectively. As N_{fc} and N_{ac} increase, both the I_{on} and I_{off} decrease gradually. This is because, whether it is the fixed charge or the acceptor-type trap, a certain amount of charge is generated at the DE/channel interface, which could influence the charges originally generated in the channel by the V_g. In addition, this change affects the FE polarization [4, 5], which could further affect the total charges at the interface. It is found that the I_{off} varies faster than the I_{on}, which could probably be due to the fact that the total charges at the interface itself are smaller at lower V_g. Thus, the change in the charges caused by the N_{fc} or N_{ac} have a greater impact. In contrast, the charges at the interface itself are larger at higher V_g, and the change in the charges due to the N_{fc} or N_{ac} has a smaller impact. As a result, the I_{on} variation at higher V_g is smaller than the I_{off} variation at lower V_g. By considering the N_{fc} or N_{ac} individually, the impact of the acceptor-type traps on the I_{on} is larger but on the I_{off} is smaller than that of the fixed charges. This phenomenon could be explained by the corresponding polarization (*P*) in figure 4(c), where the *P* caused by the fixed charges is larger at low $V_g = 0$ V but smaller at high $V_g = 0.8$ V than that caused by acceptor-type traps. The FE polarization as a critical factor of the FeFET can likewise explain the *SS* variation (in figure 3) caused by the interfacial charges. The shaded part with slashes in figure 4(c) represents the *P* variation with

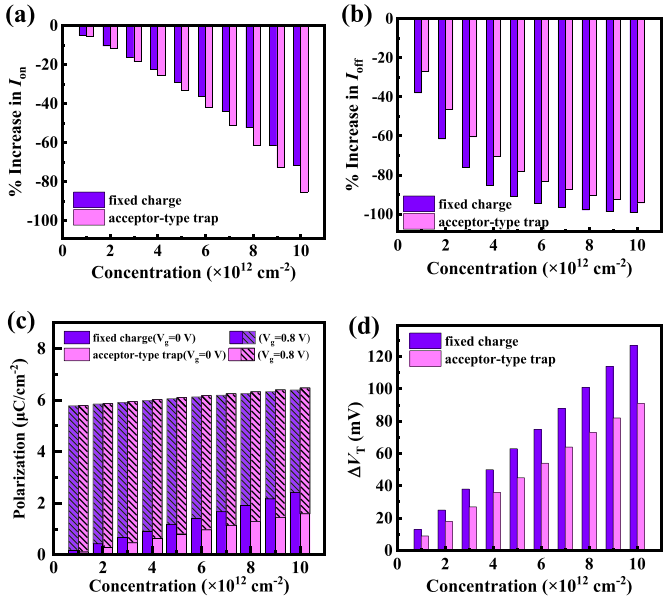

Figure 4. The change in percentage of (a) I_{on} and (b) I_{off}, (c) *P* values at $V_g = 0$ and 0.8 V with different N_{fc} and N_{ac}, and (d) the dependency between ΔV_T and N_{fc} (or N_{ac}).

the V_g varying from 0 to 0.8 V, which decreases gradually with the N_{fc} or N_{ac} increasing. This decreased *P* variation results in a decrease in the variation of the voltage across the FE layer and further a reduction in the gate voltage amplification effect, which ultimately contributes to the *SS* degradation in the FeFET. Figure 4(d) shows the dependency between the V_T and N_{fc} (or N_{ac}). It is found that the V_T offset (ΔV_T) rises approximately linearly with the N_{fc} and N_{ac} increasing. In addition, compared to the fixed charges, the acceptor-type traps exhibit a smaller impact on the V_T, which could be due to smaller variation of the charges caused by the acceptor-type traps compared to the fixed charges at the same concentration [24].

Figures 5(a)–(d) demonstrate the combined impact of the fixed charges and acceptor-type traps on the FeFET device performance including the SS_{min}, I_{on}, I_{off} and V_T. From figure 5(a), as the N_{fc} increases, the impact of the acceptor-type traps on the SS_{min} becomes greater: that is, the same variation of the N_{ac} causes a greater change in SS_{min}. This could be ascribed to the decrease in the FE polarization variation (in figure 3(c)) caused by the charges as the N_{fc} increases. Thus, it degrades the subthreshold characteristics and the NC effect

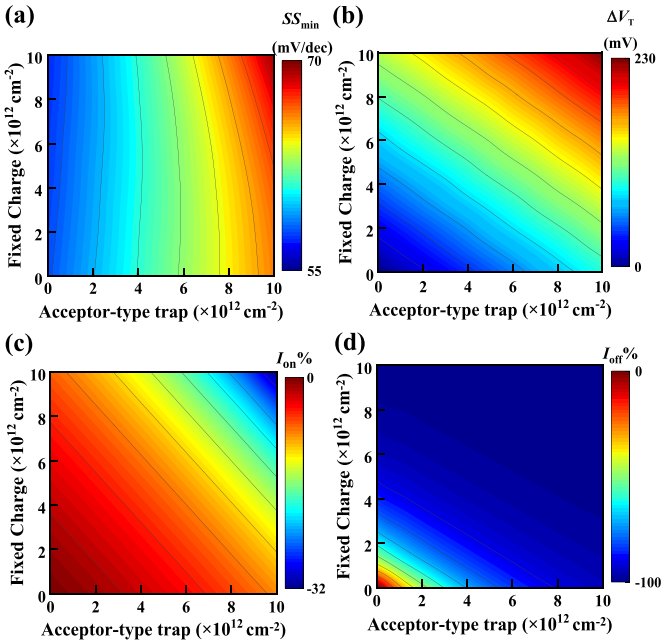

Figure 5. The combined impact of the fixed charges and acceptor-type traps on (a) SS_{min}, (b) V_T, (c) I_{on} and (d) I_{off}.

by shifting the operation point. The degraded NC effect due to the N_{fc} increase further degrades the gate controllability, resulting in an enhanced impact of the N_{ac} [27]. Similarly, as the N_{ac} increases, the impact of the fixed charges on the SS_{min} also becomes greater. Consequently, the *SS* degrades faster as the interfacial charges increase. For the V_T in figure 5(b), there is no significant interaction between the fixed charges and acceptor-type traps, except that the fixed charges have a greater impact on the V_T than the acceptor-type traps. This is because the V_T is dependent on the number of charges, and the number of charges caused by the N_{ac} and N_{fc} is individual at low V_g. For the switching current in figures 5(c) and (d), with the N_{ac} increasing, the impact of the fixed charges on the I_{on} becomes greater but on the I_{off} it becomes smaller. For the I_{on} extracted at $V_g = 0.8$ V, the *SS* at this gate bias decreases as the N_{ac} increases, resulting in a larger I_{on} variation with the same ΔV_T induced by the N_{fc} and, further, a greater impact on I_{on}. In contrast, for the I_{off} extracted at $V_g = 0$ V, the *SS* at this gate bias increases as the N_{ac} increases, resulting in a smaller I_{off} variation with the same ΔV_T induced by the N_{fc} and, further, a smaller impact on I_{off}. Similarly, with the N_{fc} increasing, the impact of the acceptor-type traps on the I_{on} also becomes greater but on the I_{off} becomes smaller. In addition, from the values of the I_{on} and I_{off} variations, it can be observed that the I_{off} is much more affected by the N_{fc} (or N_{ac}), indicating a stronger correlation between the interfacial charges and I_{off}.

Based on the above simulation analysis, it can be concluded that the device performance degradation is accelerated by the growth of the interfacial charge concentration by considering the fixed charges and acceptor-type traps simultaneously. This means that the same variation of the interfacial charge concentration has a larger influence on device performance in the high-concentration scenario compared to the low-concentration scenario. Under the co-action of the fixed charges and acceptor-type traps, the fixed charges play an important role in the V_T and I_{off}, but the acceptor-type traps become dominant in the *SS* and I_{on}. Notably, the previous discussion is based on the assumption that N_{fc} is equal to N_{ac}: namely, N_{fc} and N_{ac} are assumed to be of the same order of magnitude. In contrast, when either N_{fc} or N_{ac} is much larger than the other, the charge with larger concentration accounts for the primary contribution to the impact of the device performance, except for the *SS*. For the *SS* of the device, it is always influenced by the acceptor-type traps. Meanwhile, the charge with a larger concentration can significantly amplify the impact of the charge with the smaller concentration on the device performance, other than the V_T. Furthermore, assuming that the acceptor-type traps become residual charges after capturing the charge, it can be forecasted that the transformation of the acceptor-type traps into residual charges at low N_{ac} would result in a small change in the device performance, except for a large impact on the I_{off}. However, when the N_{ac} becomes larger, the BTI effect will gradually intensify and cause an increase in V_T and a decrease in I_{off} during the transformation process.

4. Conclusions

We study the impact of the interfacial charges including the fixed charge and acceptor-type traps at the DE/channel interface on the performance degradation in NC-FeFETs. The device performance, including *SS*, I_{on}, I_{off} and V_T by considering the impact of fixed charges and acceptor-type traps individually, is investigated. When both the fixed charges and acceptor-type traps are present at the same time, they enhance each other's influence on device performance degradation. With the equally co-existing fixed charges and acceptor-type traps, the fixed charges dominate the V_T and I_{off}, while the acceptor-type traps dominate the *SS* and I_{on}. This work may provide insight into the device physics of FeFETs.

Data availability statement

The data that support the findings of this study are available upon reasonable request from the authors.

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