

Impacts of SiO₂-Buried Structure on Performances of GaN-Based Vertical-Cavity Surface-Emitting Lasers

Rongbin Xu¹, Hidefumi Akiyama, and Baoping Zhang¹

Abstract—Numerical analysis of the optical and electrical properties of GaN-based vertical-cavity surface-emitting lasers (VCSELs) with SiO₂-buried structure were performed. The simulation results show that, as the SiO₂ layer gets thicker, threshold simply gets lower, but slope efficiency gets initially smaller and then gets larger. The mechanism of these tendencies are explained as, when the SiO₂ layer becomes thicker, a better lateral optical confinement can be achieved, while the current confinement becomes worse due to the existence of polarization electric field. Furthermore, since the injection current density is higher for VCSEL with small aperture size, the worse current confinement will result in lower slope efficiency. A proper design of SiO₂-buried structure to avoid the effect of leakage current is essentially important to achieve high-efficiency GaN-based VCSELs.

Index Terms—GaN-based laser, numerical simulation vertical-cavity surface-emitting laser (VCSEL), optical and current confinement.

I. INTRODUCTION

IN CONTRAST to edge-emitting laser diodes, some advantages of vertical-cavity surface-emitting lasers (VCSELs) were highlighted such as small mode volume, low divergent output beam, and easy array formation. These unique properties have made VCSELs ubiquitous in our daily lives, such as optical data storage, lighting, and laser printers [1], [2]. At present, GaAs-based long-wavelength infrared (IR) VCSELs have been commercialized due to its mature fabrication process. If VCSELs can extend the available emission

wavelengths into ultraviolet to visible regime, many more applications could benefit from such a light source. However, GaN-based short-wavelength VCSELs are still suffering from some challenges [3], [4].

Generally, AlGaAs-selective oxide layer employed in GaAs-based VCSELs not only achieves current confinement but also provides a stable refractive index variation in the lateral direction to improve light confinement [5]. GaAs-based VCSELs are very sensitive to this selective oxide structure. Changing the diameter, position, and the thickness of oxide layers may significantly influence the device performance. Therefore, the design and optimization of oxide-confined structure had been carried out extensively in experiment and theory [6], [7], [8], [9]. In comparison, selective oxidation is very difficult in GaN-based VCSELs due to the character of the material itself. In order to realize lateral current confinement in current injection GaN-based VCSELs, in general, a patterned insulating layer is deposited directly on the surface of p-GaN. However, this method will result in a convex shape structure, which will cause lateral diffraction and radiation loss, and we called it antiguiding effect [4], [10], [11]. In recent years, many research groups have developed various approaches to achieve better lateral confinement structure in GaN-based VCSELs by using ion implantation [12], [13], photoelectrochemically etched air-gap aperture [14], buried insulating layer [15], [16], [17], monolithic curved mirror [18], and reactive ion etching (RIE) passivation [19], [20]. Among them, insulator-buried structure is rather simple and preferable. The insulator-buried structure could not only provide good electrical confinement but also improve the optical confinement in the transverse direction. In 2018, Kuramoto et al. [15] introduced a SiO₂-buried structure in GaN-based VCSEL with hybrid epitaxial/dielectric distributed Bragg reflector (DBR). The reported devices showed a high output power of 6 mW. The next year, they applied the same structure in 256-element blue VCSEL array and achieved a high output power of 1.19 W [21]. In our previous work, we also experimentally found that SiO₂-buried structure can effectively reduce the intracavity loss and improve the performance of GaN-based VCSELs [17]. However, this structure still lacks detailed study, and further investigation is required for its future practical use.

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Rongbin Xu and Baoping Zhang are with the Department of Microelectronics and Integrated Circuits, Optoelectronics Laboratory of Micro/nano-Optoelectronics, Xiamen University, Xiamen 361005, China (e-mail: bzhang@xmu.edu.cn).

Hidefumi Akiyama is with the Institute for Solid State Physics, The University of Tokyo, Kashiwa, Chiba 277-8581, Japan.

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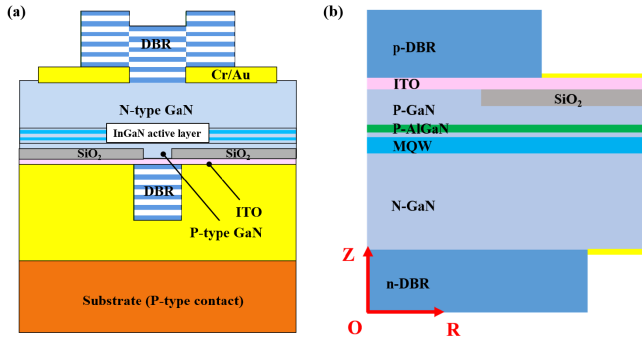


Fig. 1. (a) Schematic cross section of the GaN-based VCSEL with SiO₂-buried structure. (b) Simulation structure of resonant cavity, O, Z, and R, represent the original point, the vertical, and lateral coordinate of simulation model, respectively.

TABLE I
DETAIL LAYER STRUCTURE OF THE CALCULATED VCSEL

Material	Thickness (nm)	Doping concentration (cm ⁻³)
Ta ₂ O ₅ /SiO ₂	10 × 50.93/78.77	--
n-GaN	1994.5	2.5 × 10 ¹⁸
In _{0.02} Ga _{0.98} N	85	--
In _{0.18} Ga _{0.82} N/GaN	2 × 2.5/6	--
In _{0.03} Ga _{0.97} N	85	--
p-Al _{0.18} Ga _{0.82} N	20	1 × 10 ¹⁸
p-GaN	596	4 × 10 ¹⁷
SiO ₂	20	--
ITO	40	--
SiO ₂ /Ta ₂ O ₅	12 × 78.77/50.93	--

In this article, we have theoretically investigated both optical and electrical properties of GaN-based VCSEL with SiO₂-buried structure. The simulation results showed that the threshold current and slope efficiency of GaN-based VCSEL are remarkably impacted by modifying the SiO₂ thickness. However, the variation tendencies are different. When the SiO₂ layer becomes thicker, a better lateral optical confinement can be achieved, while the current confinement becomes worse. In addition, since the current injection area is also determined by SiO₂ layer, the devices with different aperture sizes were also investigated. This study provides reference significance for the realization of high-performance GaN-based VCSEL.

II. DEVICE STRUCTURE AND PHYSICAL MODEL

The geometry of the VCSEL is schematically illustrated in Fig. 1 and the detailed layer structure is summarized in Table I. The active region consists of two In_{0.18}Ga_{0.82}N/GaN quantum wells (QWs) having a well and barrier thickness of 2.5 and 6 nm, respectively. A 20 nm Al_{0.2}Ga_{0.8}N layer was used as electron blocking layer. The VCSEL has a dual dielectric DBR design, combining the ITO current spreading layer and SiO₂ insulating layer together. The studied VCSEL has the cavity length of $\sim 16\lambda$ and the current aperture with a diameter of 15 μm is defined by SiO₂.

To investigate the electrical and optical characteristics of SiO₂-buried structure VCSEL, an advanced simulator Crosslight PICS3D was utilized in this study. The PICS3D is based on 3-D finite element analysis and can be employed

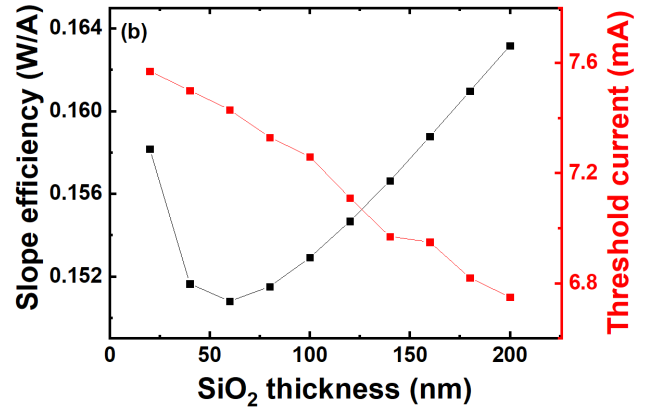
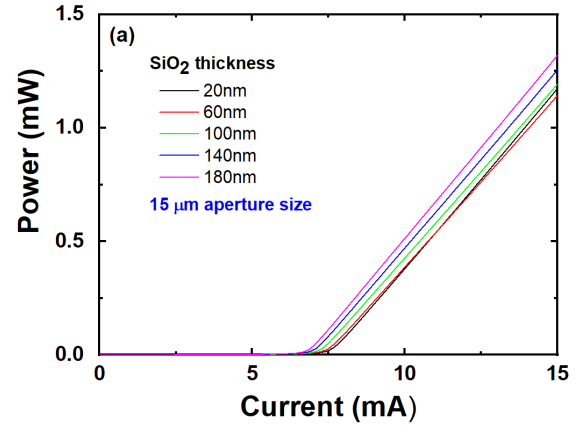


Fig. 2. (a) Simulated lasing power as a function of the injection current for devices with different SiO₂ thickness. (b) Slope efficiency and threshold current as a function of the buried SiO₂ thickness at the current of 15 mA.

to solve the Poisson's equation, current continuity equations, carrier transport equations, complex wave equations, and rate equations of VCSEL devices in the cylindrical coordinates. The transport model includes drift and diffusion of electrons and holes, Fermi statistics, as well as spontaneous and defect-related Shockley—Read—Hall (SRH) recombination of carriers. The spontaneous and piezoelectric polarization in GaN-based materials were considered in the simulator to calculate the built-in polarization field. The polarization charge density is calculated to be around $-1.2 \times 10^{13} \text{ cm}^{-2}$ [23], and the polarization level was set to 20% since the reduction of the interface charge may be screened by defects and other effects during the actual epitaxial growth and device fabrication. In the optical mode model, both the longitudinal and transverse optical modes are solved by the effective index model (EIM). The use of EIM model is beneficial to the device with complex structural variation in lateral direction. Since the cylindrical symmetry of the calculated VCSEL, the simulation model can be simplified into a 2-D axisymmetric structure, as shown in Fig. 1(b).

III. SIMULATION RESULTS AND DISCUSSION

The $P-I$ curves of 15 μm aperture size VCSELs with different SiO₂ thickness are shown in Fig. 2(a). The fitting slope efficiency and threshold current are shown in Fig. 2(b). We can observe that the threshold current slightly decrease with the

increase of SiO₂ thickness. In addition, it is interesting that the fitting slope efficiency first decreases and then increases when increasing SiO₂ thickness. The simulation results show that GaN VCSELS with SiO₂-buried structure are sensitive to the thickness of SiO₂ layer, which is the same as oxide-confined GaAs VCSELS. The trends of threshold and slope efficiency can be attributed to the influence of different SiO₂ thickness on the lateral optical and current confinement capacity of devices, which will be discussed in the latter part of the article.

A. Lateral Optical Confinement

In VCSEL structure, the threshold condition and slope efficiency are strongly dependent on the lateral optical losses. Usually, the lateral optical confinement capacity of VCSEL can be estimated by using EIM [22]. The relative refractive index difference $\Delta n/n$ can be estimated from the local resonance wavelength shift between the center and peripheral region of the VCSEL mesa, as described by the following equation:

$$\frac{\lambda_c - \lambda_p}{\lambda_c} = \frac{\Delta\lambda}{\lambda_c} = \frac{\Delta n}{n} \quad (1)$$

where λ_c and λ_p are the resonance wavelengths of the center and peripheral areas, respectively. λ_c and λ_p can be obtained from the calculated reflectivity spectrum of an entire VCSEL cavity by transfer matrix simulation. Fig. 3(a) shows the calculated $\Delta n/n$ values for SiO₂-buried structure VCSELS at the central resonance wavelength of 445 nm as a function of SiO₂ thickness. It was found that the $\Delta n/n$ gradually increase with the increase of SiO₂ thickness. Fig. 3(b) shows the fundamental (LP₀₁) and first order (LP₁₁) optical modes within the QW of the devices with different SiO₂ thickness. The full width at half maximum (FWHM) of LP₀₁ and LP₁₁ mode distributions in the lateral direction were narrowed with the increase of SiO₂ thickness. This is because the increased $\Delta n/n$ leads to a better confinement to the optical modes. The theoretical Q value of lasers can be calculated by using the method reported in [24]. And the calculated Q value of VCSEL is increase from 1000 to 2356 with the increase of SiO₂ thickness. All these suggest that a better optical confinement scheme can be achieved when the SiO₂ layer becomes thicker, and finally achieved a lower threshold current and higher slope efficiency. However, it is important to note that a thicker SiO₂ layer may not always be better for VCSEL performance. With the increase of $\Delta n/n$, the strong guiding structure ($\Delta n > 0.03$) can cause an increase of diffraction loss [10], [11]. Thus, a moderate SiO₂ thickness ($\Delta n \approx 0.03$) is usually preferred in actual device design.

B. Lateral Current Confinement

In order to investigate the underlying mechanism of varying slope efficiency, we further discuss the lateral current confinement capacity of VCSEL with different SiO₂ thickness. Fig. 4 shows the lateral distributions of hole concentrations in p-GaN below the SiO₂ layer. As shown in Fig. 4, the accumulation of holes will be formed at the p-GaN/SiO₂ interface near the edge of current aperture. This accumulation effect becomes more

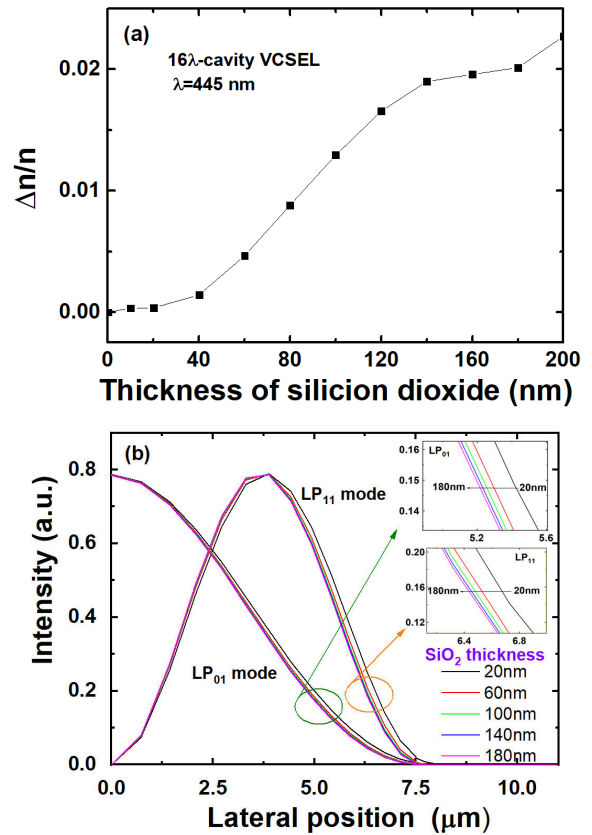


Fig. 3. (a) Relative refractive index difference as a function of SiO₂ thickness. (b) Optical mode distributions of LP₀₁ and LP₁₁ within the QW along the lateral direction. Insets show the zoom-in mode distributions curves of LP₀₁ and LP₁₁.

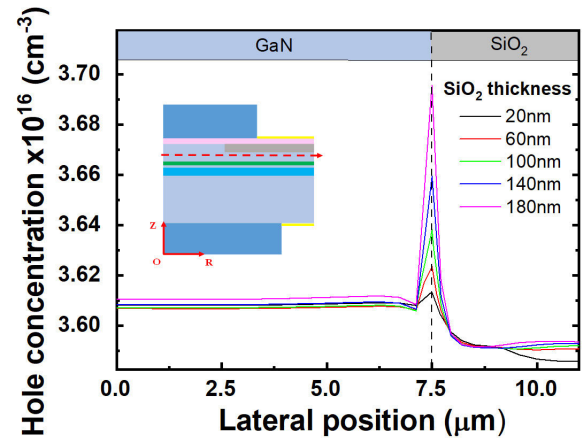


Fig. 4. Lateral hole concentrations in p-GaN below the SiO₂ layer at the current of 15 mA. The position is marked by red dashed line in the inset schematic VCSEL.

obvious when the SiO₂ layer becomes thicker. The SiO₂/GaN structure in VCSEL will form a MOS-like heterostructure [25], and the difference in the polarization across the heterointerface will result in interface charge. It has been reported that the electrical properties of the MOS SiO₂/GaN structures could be affected by the existence of polarization charge on SiO₂/GaN interface [25], [26]. Thus, the accumulation of holes could be

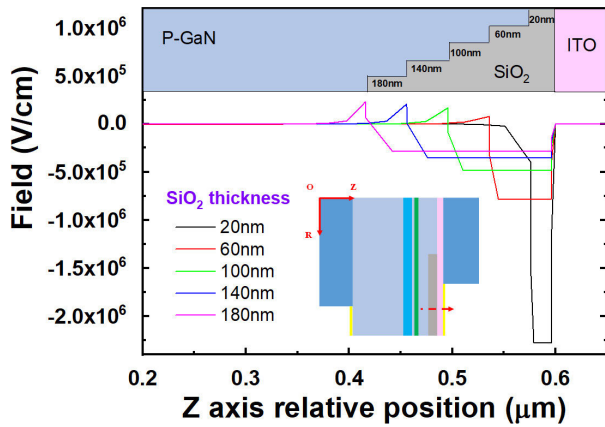


Fig. 5. Vertical electric field profiles for the VCSELs with different SiO₂ thickness. The position is marked by red dashed line in the inset schematic VCSEL.

attributed to the existence of polarization-induced electric field at the p-GaN/SiO₂ interface.

Fig. 5 shows vertical electric field profiles for the VCSELs with different SiO₂ thickness. The electric fields at the p-GaN/SiO₂ interface originate from applied bias and material polarization. The electric fields induced by applied bias and polarization are in opposite direction. When the SiO₂ thickness is thin (20 nm), the potential difference between SiO₂ layer is small, and thus the electric field originated from bias voltage can compensate the polarization electric field at the p-GaN/SiO₂ interface. However, when the SiO₂ layer becomes thicker, the potential difference becomes larger, the shielding of the polarization electric field at the p-GaN/SiO₂ interface is weakened. The unshielded polarization electric field at the p-GaN/SiO₂ interface will lead to the accumulation of holes below the SiO₂ layer, and thus led to the generation of leakage current. This leakage current is comprised of holes moving horizontally outward away from the center axis of the VCSEL, in the p-GaN layer, as shown in Fig. 6. This is the reason why the slope efficiency of VCSEL showed decrease when the thickness of SiO₂ layer is increased from 20 to 60 nm shown in Fig. 2(b). With even thicker SiO₂, the slope efficiency is improved. This is because the slope efficiency of VCSEL is affected by the injection efficiency and intracavity loss. Since the existence of leakage current, the injection efficiency first decreases with the increase of SiO₂ thickness, and thus the slope efficiency decreases. However, the thick SiO₂ layer can enhance lateral optical confinement, and the lateral optical loss can be reduced. Therefore, the slope efficiency of the simulated device showed first decrease and then increase, as shown in Fig. 2(b).

C. Effect of SiO₂ Aperture Size

In addition to the thickness of SiO₂, the current injection region is also determined by the patterned SiO₂ layer. In this part, the influence of current aperture size on the performance of SiO₂-buried structure VCSEL is considered.

Fig. 7 shows the spatial distributions of the current density (red lines), LP₀₁ and LP₁₁ mode distributions of the devices with 10 and 15 μm aperture diameters. As shown in Fig. 7, the

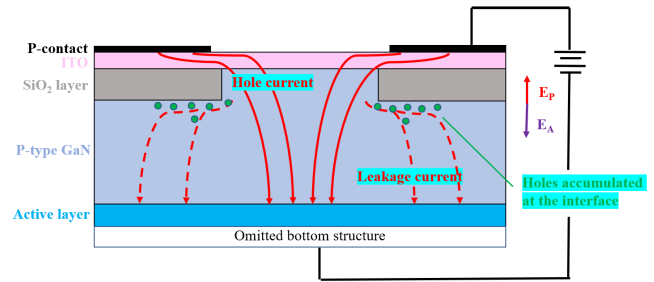


Fig. 6. Cartoon diagram illustrating hole leakage current outside the edge of current injection aperture in VCSEL. E_P and E_A are polarization and applied bias-induced electric field, respectively.

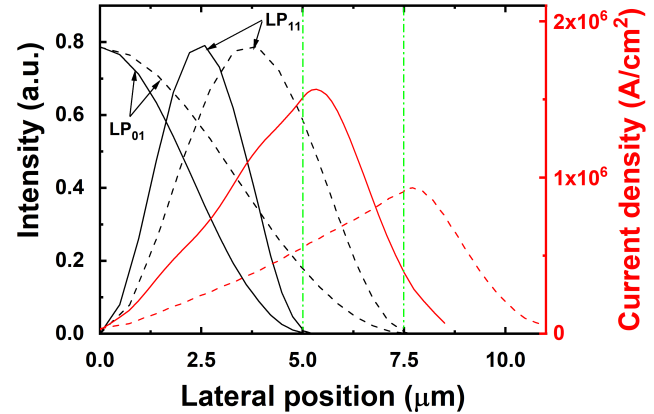


Fig. 7. Current density (red line) and optical mode (black line) distributions within the QWs along the lateral direction. The solid and dashed lines represent the VCSELs with 10 and 15 μm aperture diameters, respectively.

buried SiO₂ layer will cause current crowding, and the current density is maximized near the edge of the current injection aperture. Outside the current injection aperture, the current in QWs is comprised of the polarization-induced current and horizontal current diffusion. Since the high-order modes are distributed in the peripheral region of aperture, the nonuniform distribution of current density within the QW may favor higher order modes in such a confinement structure. However, due to the long-cavity structure and mode competition, higher order modes are suppressed and almost have no impact on the total slope efficiency, only LP₀₁ and LP₁₁ modes were considered during the simulation.

Fig. 8 shows the calculated $P-I$ curves of LP₀₁ and LP₁₁ optical modes for the VCSELs with 10 and 15 μm aperture diameters. Two transverse modes can lase simultaneously for both devices. The increasing rate of LP₁₁ mode is higher than that of LP₀₁ mode due to the nonuniform current distribution, as shown in Fig. 7. It is obviously that the devices with 10 μm aperture size have small threshold current due to the higher injection current density.

We further compare the slope efficiency of lasing modes for the devices with 10 and 15 μm aperture sizes, as shown in Fig. 9. The slope efficiency variation tendencies of LP₀₁ and LP₁₁ modes are the same as that in Fig. 2(b). The device with small (10 μm) aperture size has a low slope efficiency. In addition, contrast to the device with 20 nm SiO₂ layer, the slope efficiency of LP₀₁ and LP₁₁ modes for 15 μm aperture

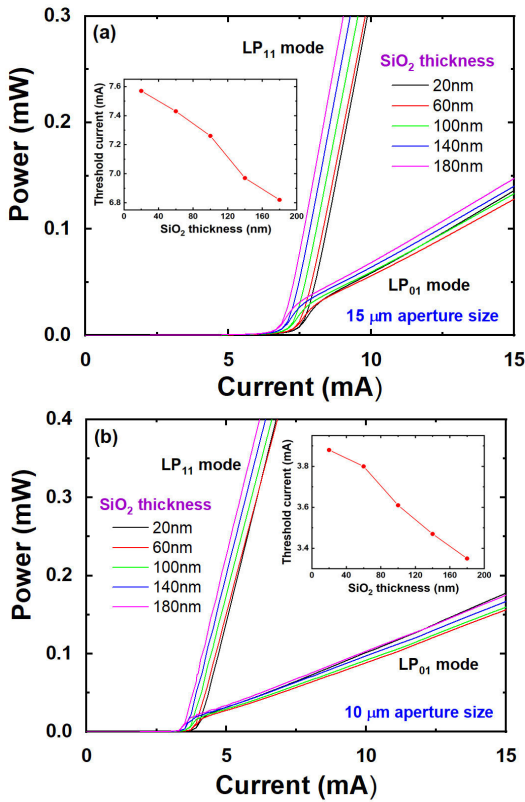


Fig. 8. P - I curves of LP₀₁ and LP₁₁ lasing modes for the devices with different SiO₂ thickness. (a) 15 μm aperture size. (b) 10 μm aperture size. Insets show the threshold current in terms of the SiO₂ thickness.

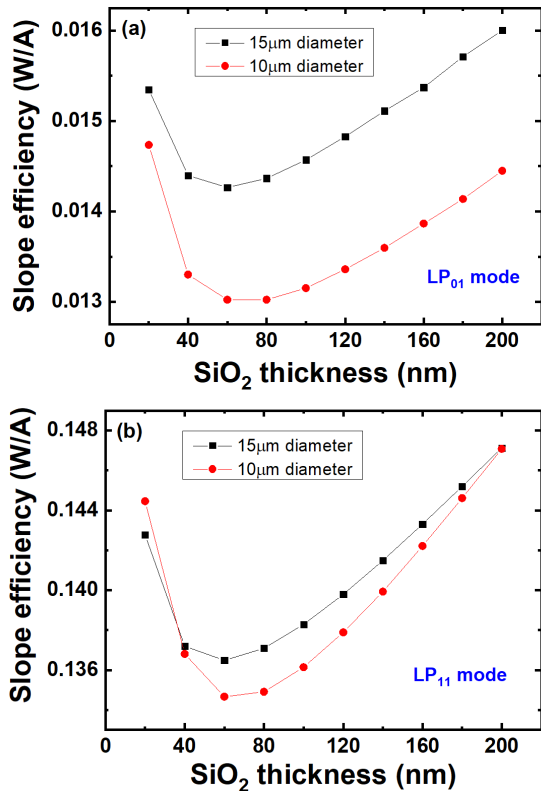


Fig. 9. Slope efficiency of (a) LP₀₁ mode and (b) LP₁₁ mode as a function of SiO₂ thickness of the devices with 10 and 15 μm aperture sizes.

size device with 60 nm SiO₂ are decreased by 7.1% and 4.4%, respectively, while the 10 μm aperture size devices

are decreased by 11.6% and 6.8%. Since injection current is concentrated distribution at the edge of the aperture, the LP₀₁ mode is more susceptible to the leakage current. Therefore, because of the higher injection current density, the leakage current has a bigger influence on the SiO₂-buried structure VCSEL with small aperture size, especially for the LP₀₁ lasing mode.

IV. CONCLUSION

In conclusion, this work provides a deeper understanding on the influence of SiO₂ layer in GaN-based VCSELS with SiO₂-buried structure. The threshold condition and the slope efficiency of VCSEL is strongly dependent on the lateral optical and current confinement caused by the SiO₂ layer. We have found that a better optical confinement scheme can be achieved when the SiO₂ layer becomes thicker. However, due to the special polarization property of GaN material, thick SiO₂ layer will lead to the accumulation of holes at the p-GaN/SiO₂ interface, resulting in leakage current. As a consequence, the slope efficiency of device exhibits an abnormal trend of decreasing initially and then increasing when the SiO₂ becomes thicker. Moreover, the variation of slope efficiency is more significant since the current density is larger for VCSELS with small aperture size. Therefore, it is important that a proper design of SiO₂ layer in VCSEL with SiO₂-buried structure is needed to avoid the effect of leakage current, especially for device with small aperture size. This work provides important significance for the development of high-performance GaN-based VCSELS.

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